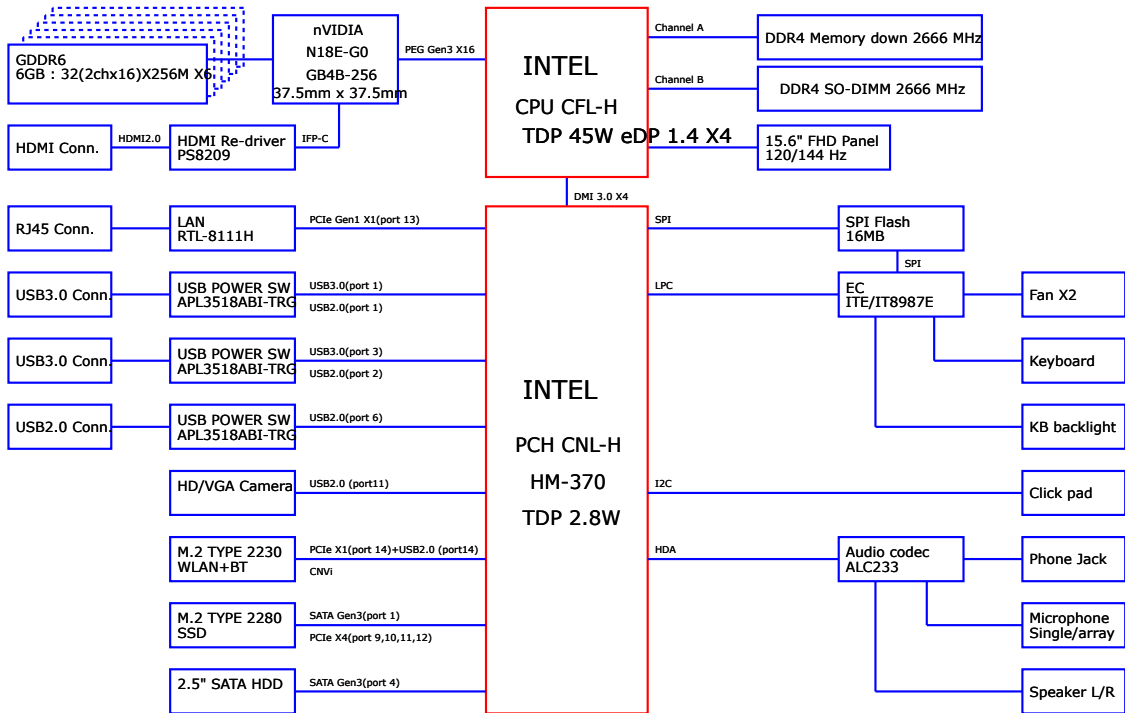
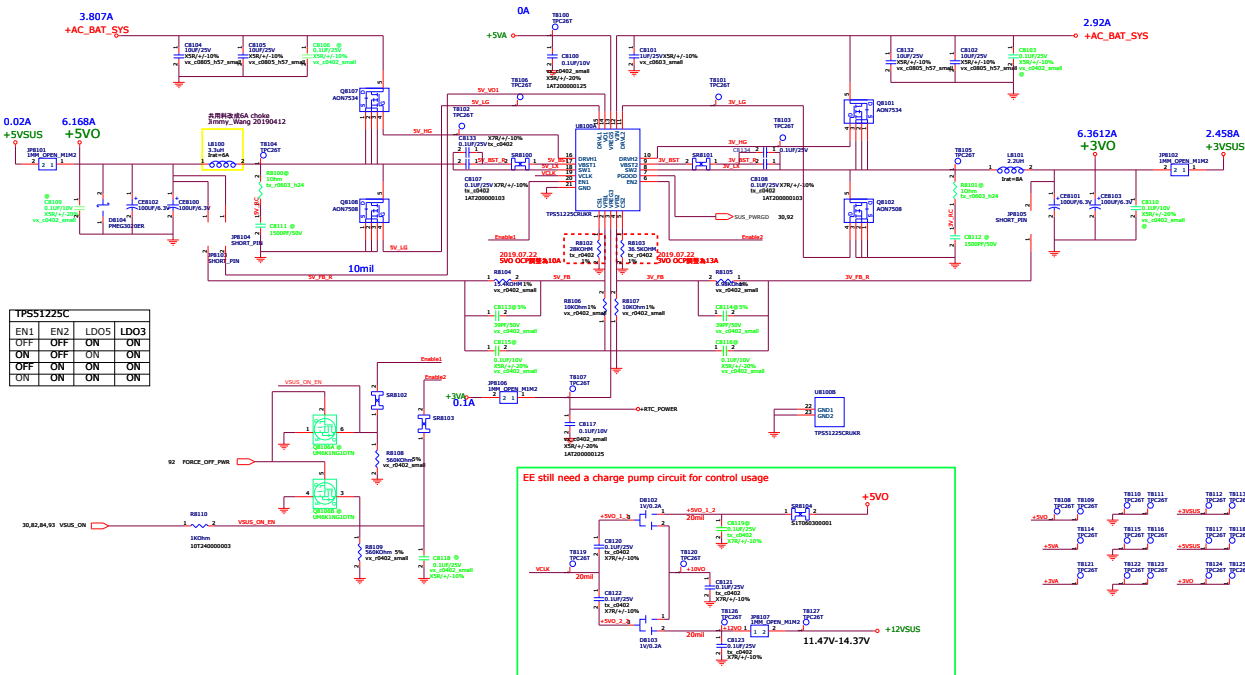


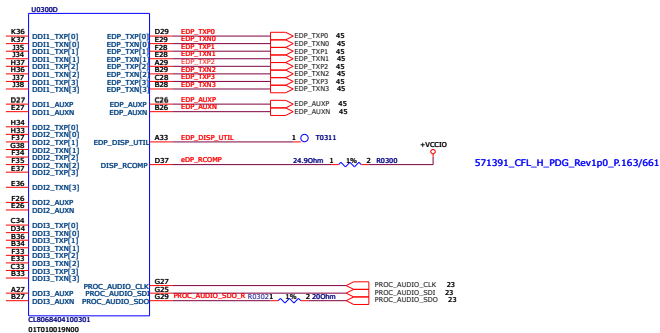
FX505GU Block Diagram

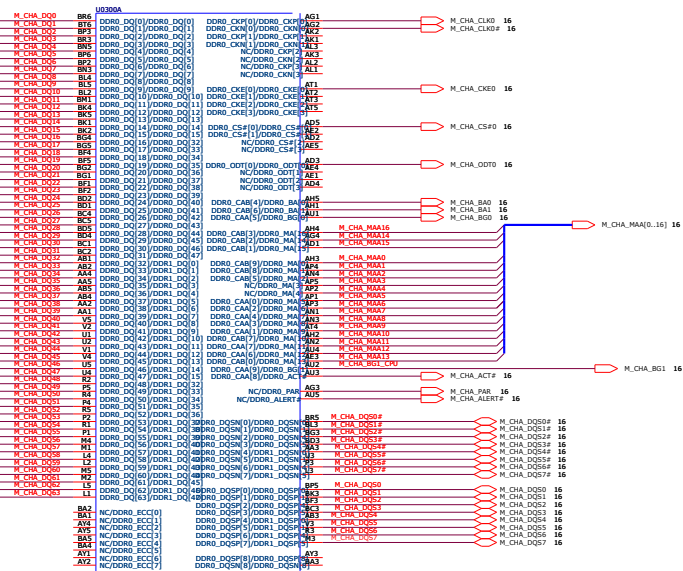


+5V0 & +3V0 POWER SUPPLY









PEGATRON		Title : D084 A	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG3-1HW RDC-1HW2-HW RD Dept.1		Engineer: XMAN	
Size A3	Project Name FXS05GE	4	99
Date:	Thursday, September 05, 2019	Sheet	of

+VCCIO 3,7,10,94

70 PCIEB_R0XN[15:0]
70 PCIEB_R0XP[15:0]

PEG Lane reversal

PCIEG_TXN[15:0] 70
PCIEG_TXP[15:0] 70

PCIEB_R0XP15	E25	U0300C	PCIEG_TXP15_C	C0501	2	1	0.22uF/6.3V	PCIEG_TXP15
PCIEB_R0XN15	D25	PEG_RXP(0)	PCIEG_TXN15_C	C0502	2	1	0.22uF/6.3V	PCIEG_TXN15
PCIEB_R0XP14	E24	PEG_RXP(1)	PCIEG_TXP14_C	C0503	2	1	0.22uF/6.3V	PCIEG_TXP14
PCIEB_R0XN14	D24	PEG_RXN(1)	PCIEG_TXN14_C	C0504	2	1	0.22uF/6.3V	PCIEG_TXN14
PCIEB_R0XP13	E23	PEG_RXP(2)	PCIEG_TXP13_C	C0505	2	1	0.22uF/6.3V	PCIEG_TXP13
PCIEB_R0XN13	D23	PEG_RXN(2)	PCIEG_TXN13_C	C0506	2	1	0.22uF/6.3V	PCIEG_TXN13
PCIEB_R0XP12	E22	PEG_RXP(3)	PCIEG_TXP12_C	C0507	2	1	0.22uF/6.3V	PCIEG_TXP12
PCIEB_R0XN12	D22	PEG_RXN(3)	PCIEG_TXN12_C	C0508	2	1	0.22uF/6.3V	PCIEG_TXN12
PCIEB_R0XP11	E21	PEG_RXP(4)	PCIEG_TXP11_C	C0509	2	1	0.22uF/6.3V	PCIEG_TXP11
PCIEB_R0XN11	D21	PEG_RXN(4)	PCIEG_TXN11_C	C0510	2	1	0.22uF/6.3V	PCIEG_TXN11
PCIEB_R0XP10	E20	PEG_RXP(5)	PCIEG_TXP10_C	C0511	2	1	0.22uF/6.3V	PCIEG_TXP10
PCIEB_R0XN10	D20	PEG_RXN(5)	PCIEG_TXN10_C	C0512	2	1	0.22uF/6.3V	PCIEG_TXN10
PCIEB_R0XP9	E19	PEG_RXP(6)	PCIEG_TXP9_C	C0513	2	1	0.22uF/6.3V	PCIEG_TXP9
PCIEB_R0XN9	D19	PEG_RXN(6)	PCIEG_TXN9_C	C0514	2	1	0.22uF/6.3V	PCIEG_TXN9
PCIEB_R0XP8	E18	PEG_RXP(7)	PCIEG_TXP8_C	C0515	2	1	0.22uF/6.3V	PCIEG_TXP8
PCIEB_R0XN8	D18	PEG_RXN(7)	PCIEG_TXN8_C	C0516	2	1	0.22uF/6.3V	PCIEG_TXN8
PCIEB_R0XP7	E17	PEG_RXP(8)	PCIEG_TXP7_C	C0517	2	1	0.22uF/6.3V	PCIEG_TXP7
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PCIEB_R0XN5	D15	PEG_RXN(10)	PCIEG_TXN5_C	C0522	2	1	0.22uF/6.3V	PCIEG_TXN5
PCIEB_R0XP4	E14	PEG_RXP(11)	PCIEG_TXP4_C	C0523	2	1	0.22uF/6.3V	PCIEG_TXP4
PCIEB_R0XN4	D14	PEG_RXN(11)	PCIEG_TXN4_C	C0524	2	1	0.22uF/6.3V	PCIEG_TXN4
PCIEB_R0XP3	E13	PEG_RXP(12)	PCIEG_TXP3_C	C0525	2	1	0.22uF/6.3V	PCIEG_TXP3
PCIEB_R0XN3	D13	PEG_RXN(12)	PCIEG_TXN3_C	C0526	2	1	0.22uF/6.3V	PCIEG_TXN3
PCIEB_R0XP2	E12	PEG_RXP(13)	PCIEG_TXP2_C	C0527	2	1	0.22uF/6.3V	PCIEG_TXP2
PCIEB_R0XN2	D12	PEG_RXN(13)	PCIEG_TXN2_C	C0528	2	1	0.22uF/6.3V	PCIEG_TXN2
PCIEB_R0XP1	E11	PEG_RXP(14)	PCIEG_TXP1_C	C0529	2	1	0.22uF/6.3V	PCIEG_TXP1
PCIEB_R0XN1	D11	PEG_RXN(14)	PCIEG_TXN1_C	C0530	2	1	0.22uF/6.3V	PCIEG_TXN1
PCIEB_R0XP0	E10	PEG_RXP(15)	PCIEG_TXP0_C	C0531	2	1	0.22uF/6.3V	PCIEG_TXP0
PCIEB_R0XN0	D10	PEG_RXN(15)	PCIEG_TXN0_C	C0532	2	1	0.22uF/6.3V	PCIEG_TXN0

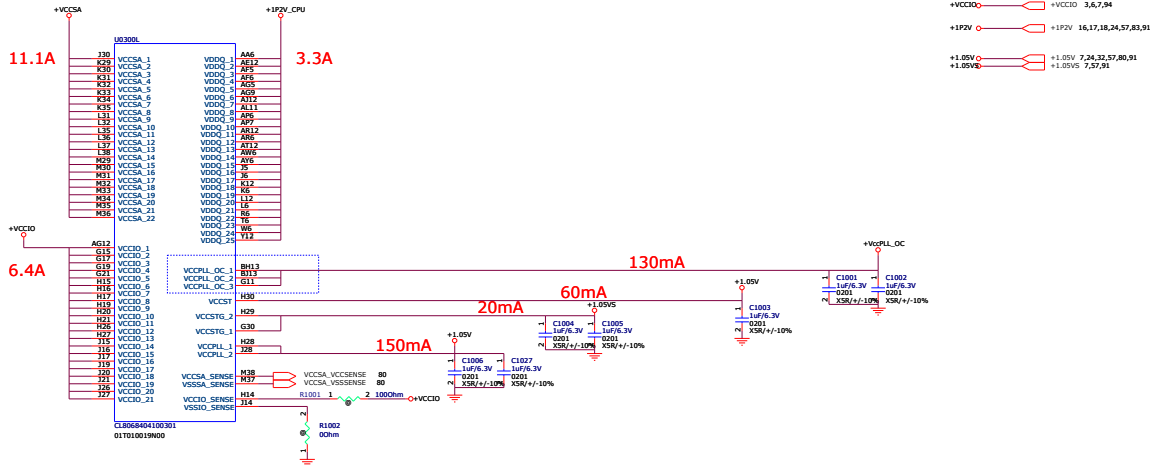
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+VCCIO R0600 1 2 24.90nm PEG_R0COMP

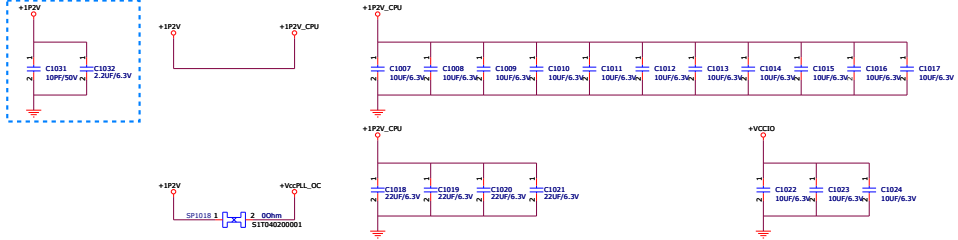
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W/S=12/15 mil, length<400mil

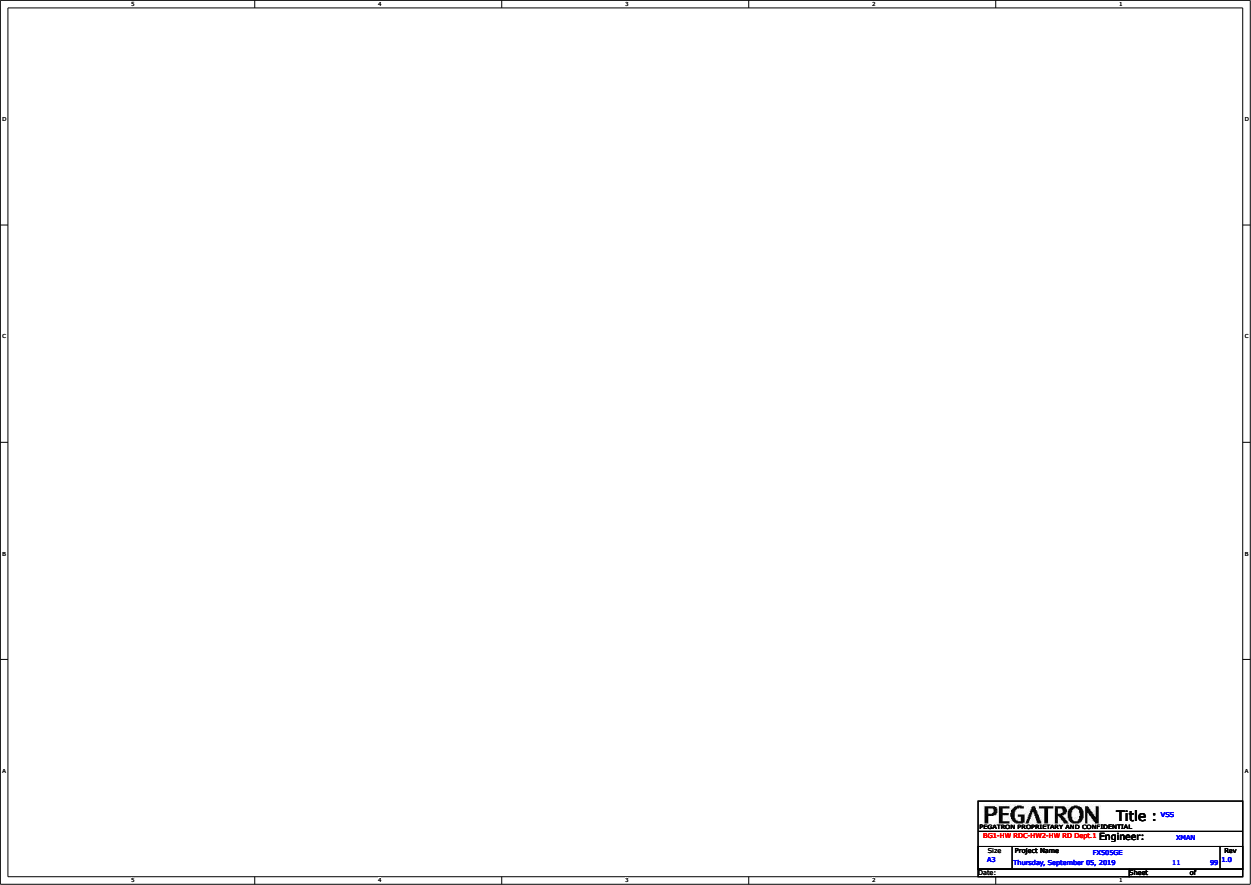
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20 DML_R0XN0	E8	DML_RXN(0)	DML_TXN0	20
20 DML_R0XP1	D6	DML_RXP(1)	DML_TXP1	20
20 DML_R0XN1	E6	DML_RXN(1)	DML_TXN1	20
20 DML_R0XP2	D5	DML_RXP(2)	DML_TXP2	20
20 DML_R0XN2	E5	DML_RXN(2)	DML_TXN2	20
20 DML_R0XP3	D3	DML_RXP(3)	DML_TXP3	20
20 DML_R0XN3	E3	DML_RXN(3)	DML_TXN3	20

C:\BSP\BSP1\BSP001
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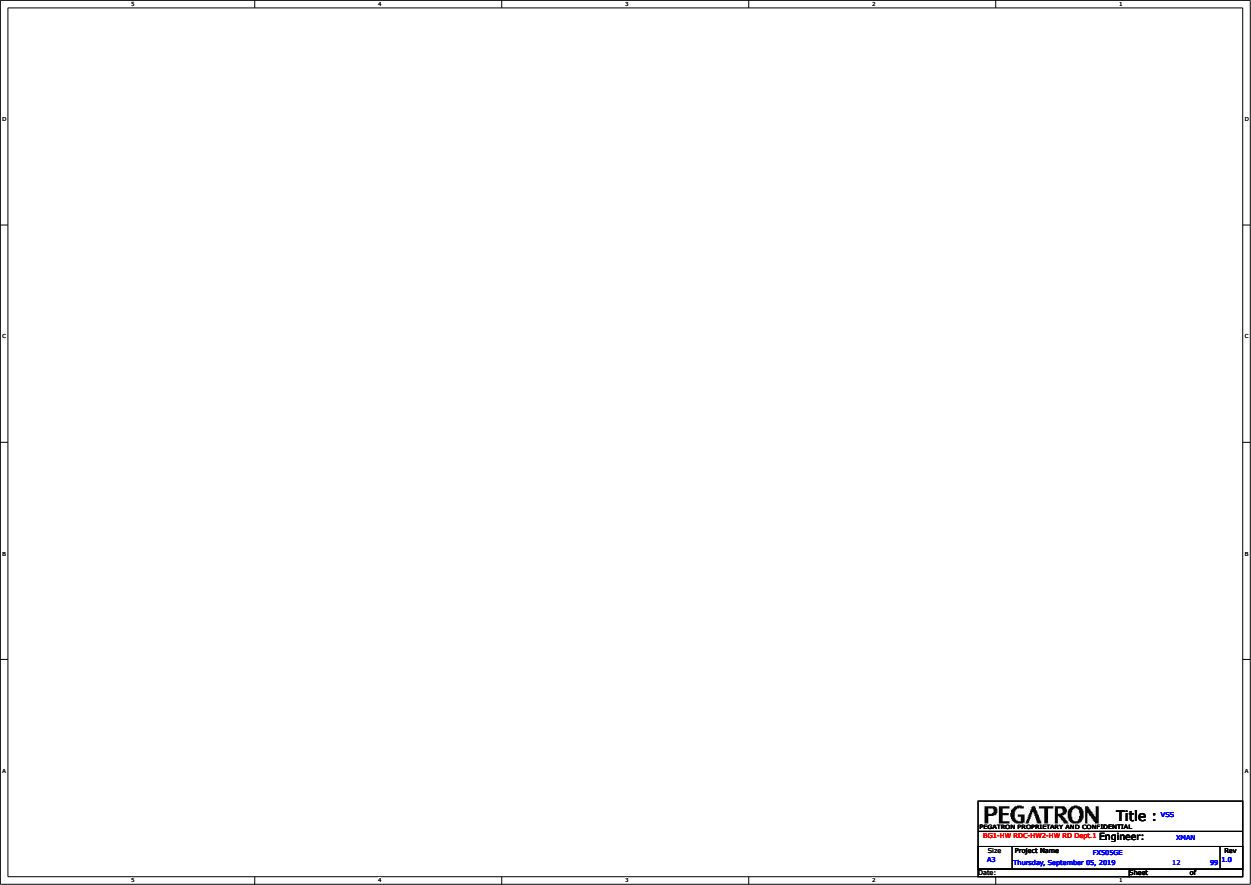


FX505 RF request @20180712

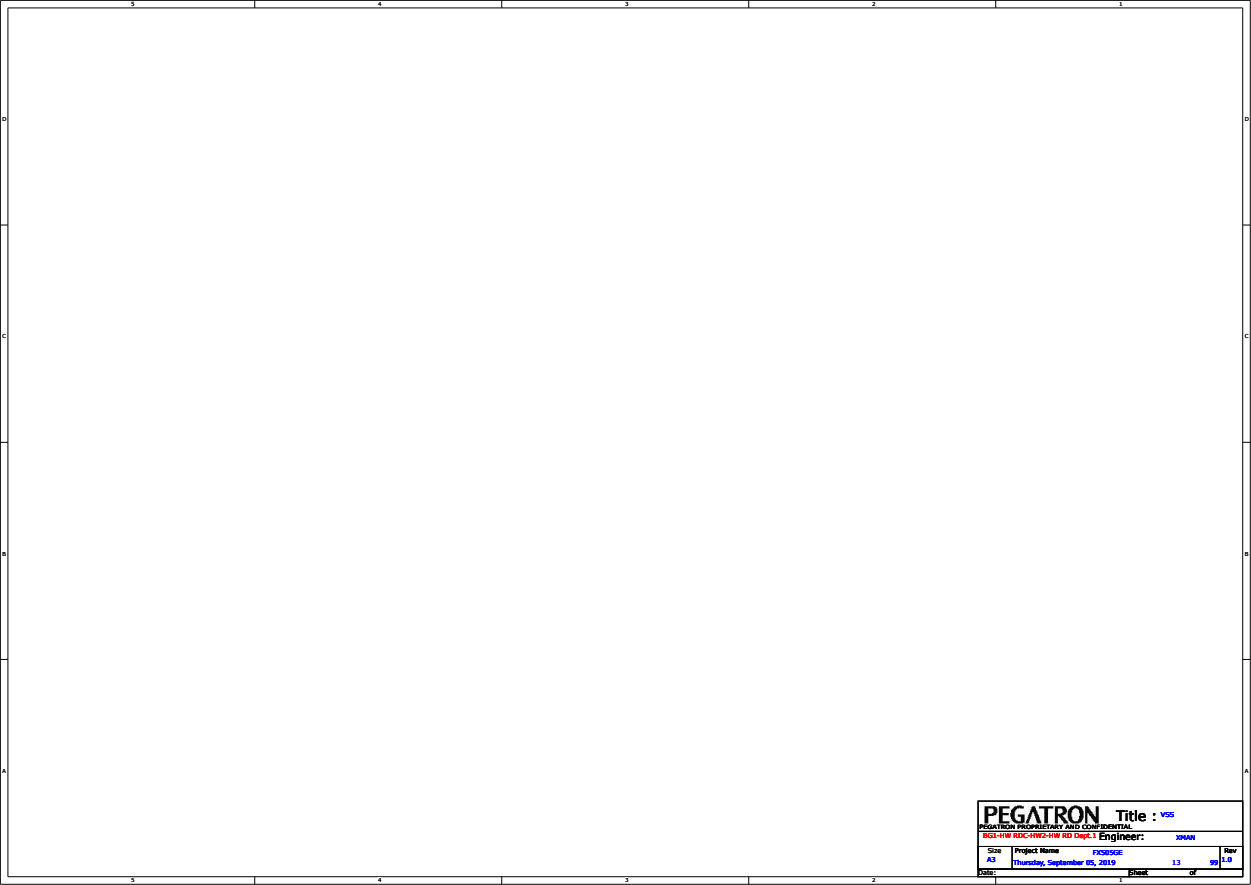




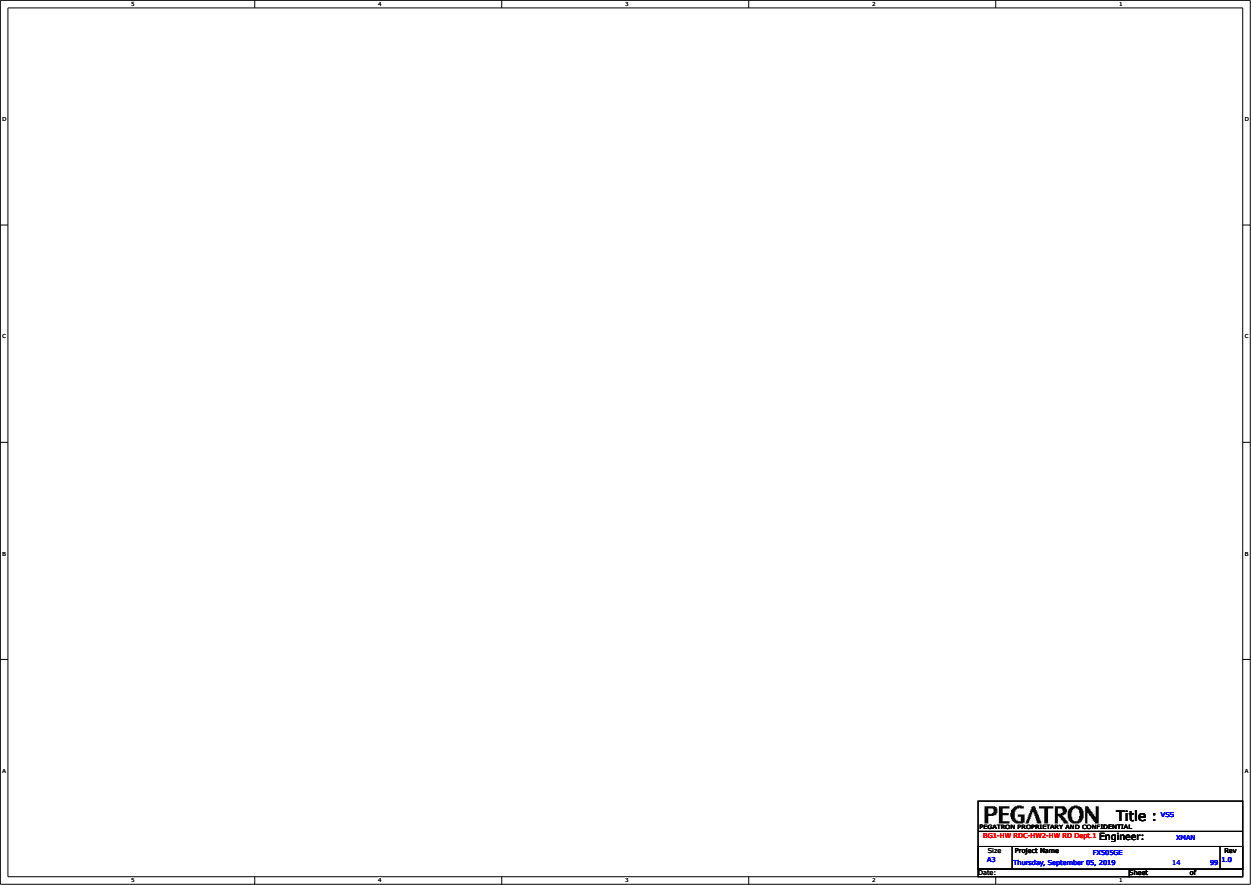
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BG3-HW RDC-HW2-HW RD Dupr.1 Engineer: XINXIN				
Size	Project Name	FXSD5DGE	Rev	
A3	Thursday, September 05, 2019	1.1	99	1.0
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PEGATRON Title : VSS				
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BG3-HW RDC-HW2-HW RD Dupr.1 J064N				
Size	Project Name	FXSD5GE	Rev	
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DATE		Sheet 1 of 99		



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PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dwg.1				
Engineer:			JOMAN	
Size	Project Name	FXSDSGE	Rev	
A3	Thursday, September 05, 2019	1.3	99	1.0
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PEGATRON

Title : VSS

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RG3-HW RDC-HW2-HW RD Dupr.1

JOHAN

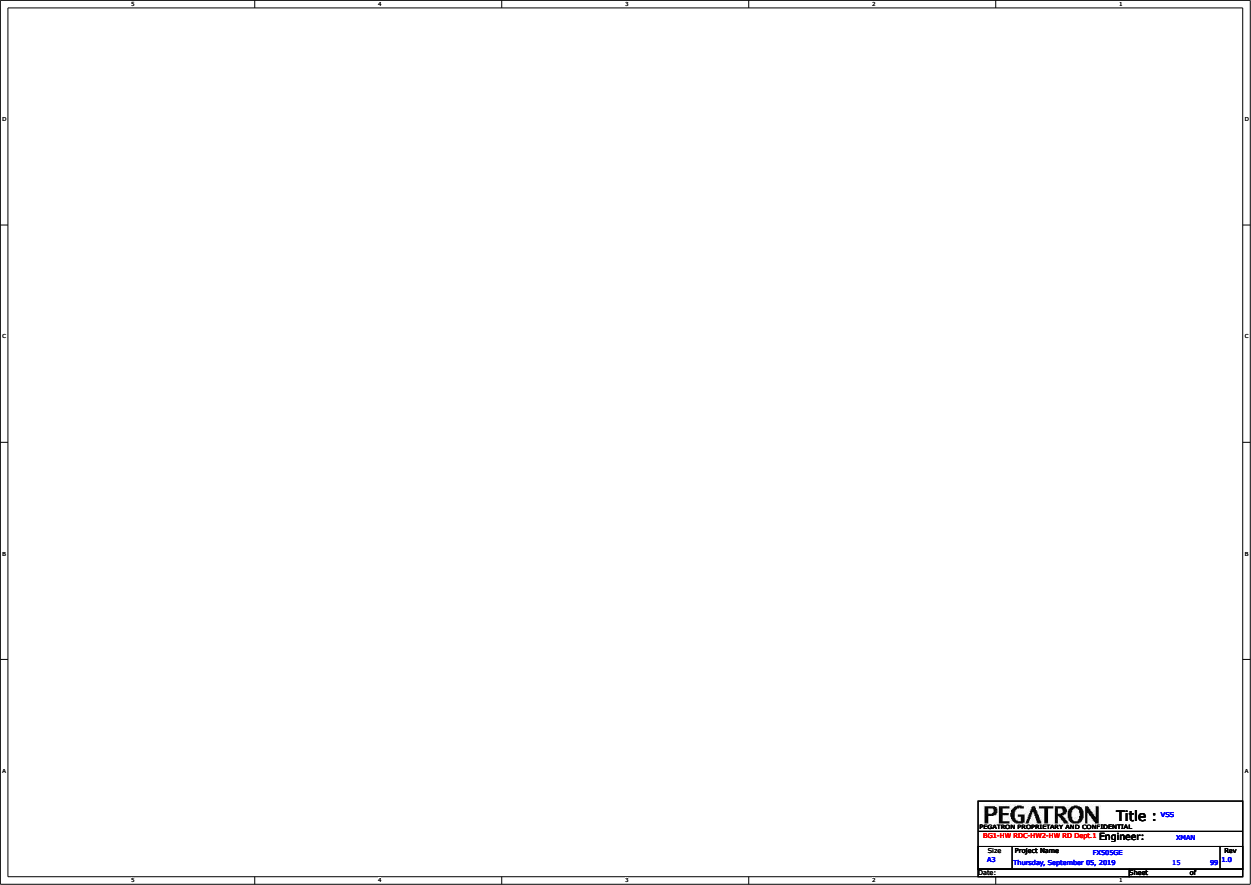
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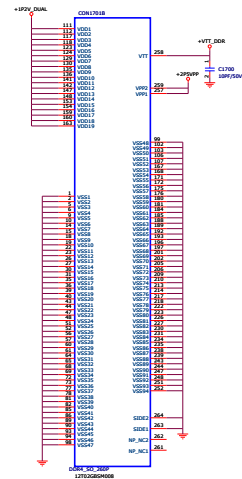
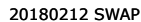
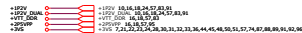
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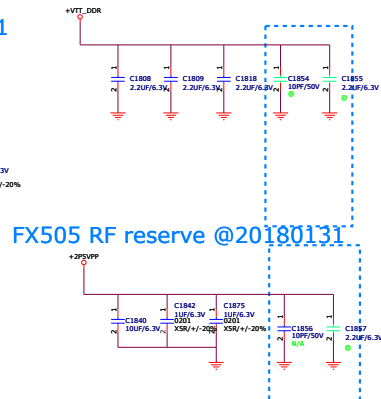
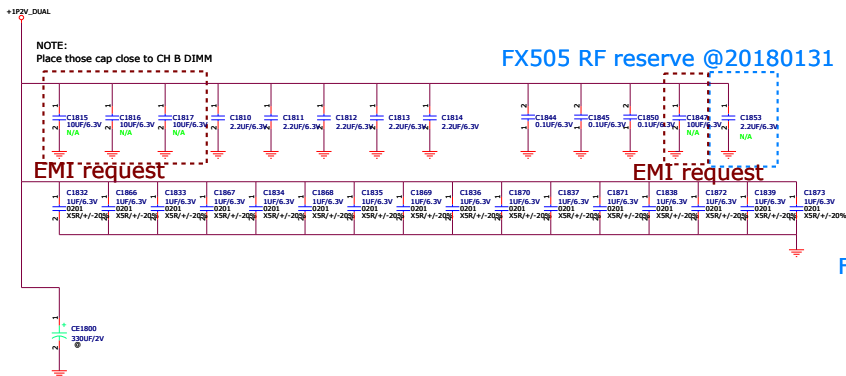
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BG3-HW RDC-HW2-HW RD Dupr.1 Engineer: XINXIN			
Size	Project Name	FXSD5DGE	Rev
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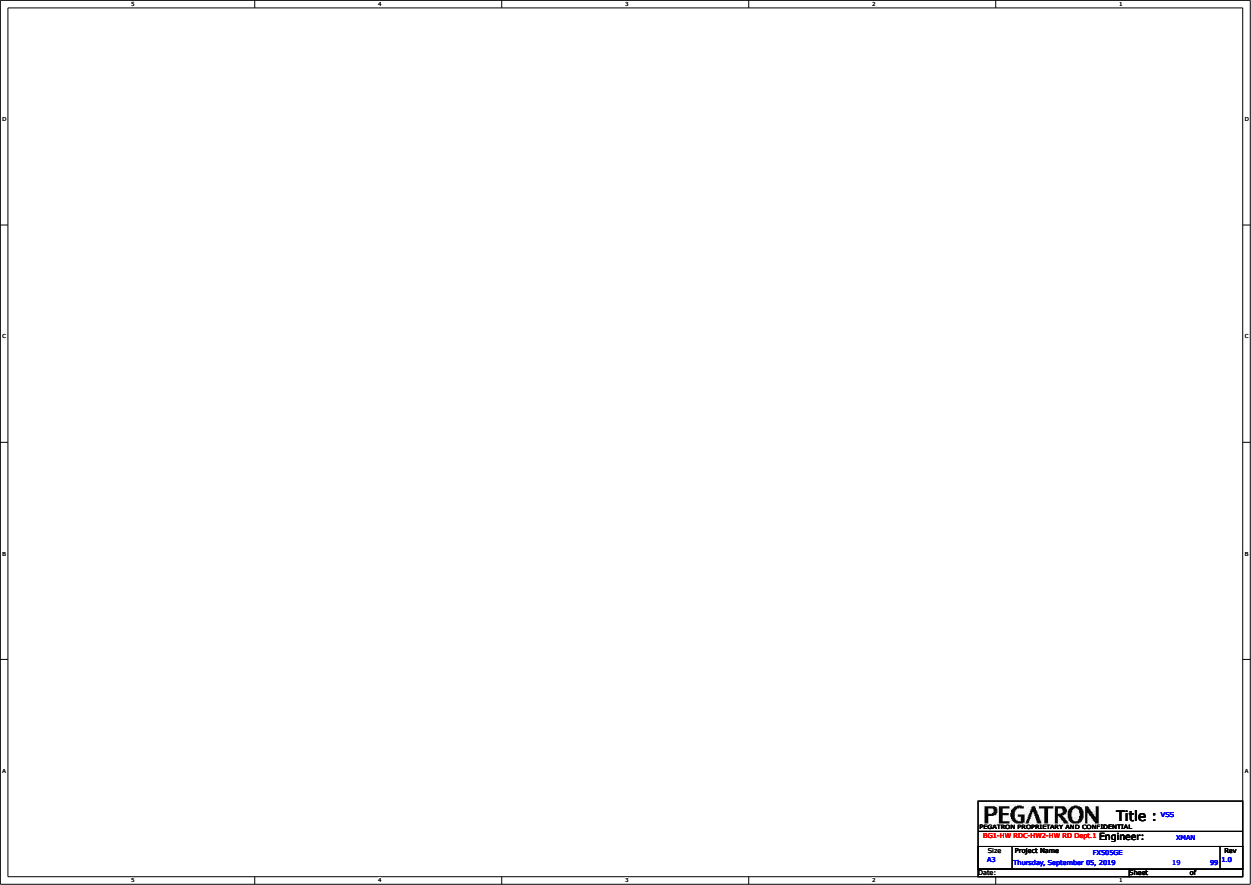


CFL-H DDR4 SODIMM Decoupling

DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)	Note
DDR4 2 Channels SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 μ F (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1 μ F (0402)	
		1 placeholder	1x 330 μ F (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10 μ F (0603)	
		Placed on VTT plane close to DIMM	4x 1 μ F (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10 μ F (0603)	
		DIMM Pin side, 1 per DIMM	2x 1 μ F (0402)	
	VDDSPD	Place close to DIMM	2x 0.1 μ F (0402)	
		Place close to DIMM	2x 2.2 μ F (0402)	

I2C_Port	Module	DEVICE	7-bit addr
I2C_0	TOUCH PAD		
I2C_1			
SMBUS	DDR Channel A(CON1601)		
	DDR Channel B(CON1701)		
SMBUS0 (EC)	BATTERY		0X0B
	CHARGE IC	BQ24780SRUYR	0X09
SMBUS1 (EC)	GPU		0X9E



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BG3-HW RDC-HW2-HW RD Dupr.1 J064N				
Size	Project Name	FXSD5GE	Rev	
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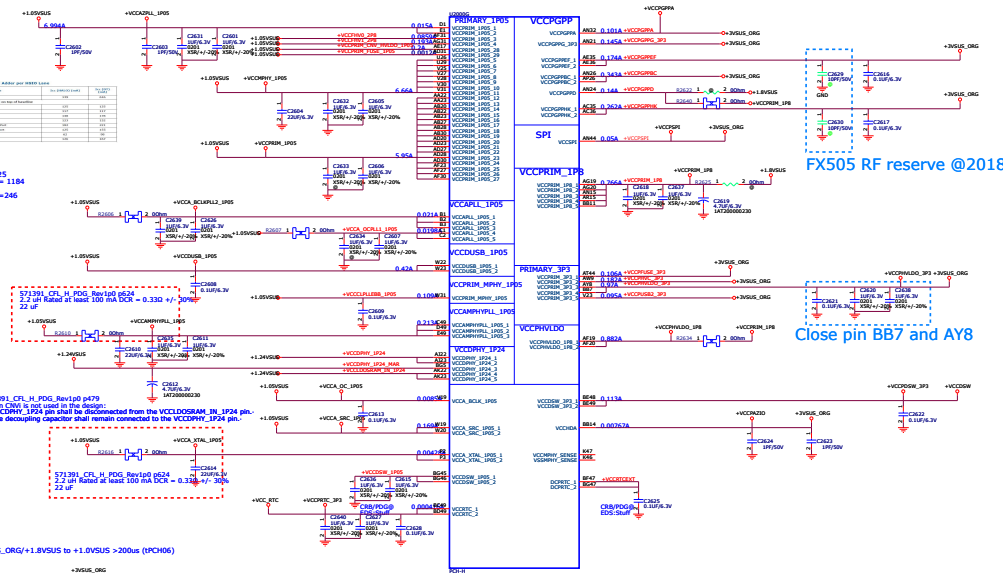


Table 1-1: Pinmux VCCPWRN_UPPER Address pin (IEEE 1598)

Pin	Function	Pin	Function
1	VCCPWRN_UPPER[0]	10	VCCPWRN_UPPER[9]
2	VCCPWRN_UPPER[1]	11	VCCPWRN_UPPER[10]
3	VCCPWRN_UPPER[2]	12	VCCPWRN_UPPER[11]
4	VCCPWRN_UPPER[3]	13	VCCPWRN_UPPER[12]
5	VCCPWRN_UPPER[4]	14	VCCPWRN_UPPER[13]
6	VCCPWRN_UPPER[5]	15	VCCPWRN_UPPER[14]
7	VCCPWRN_UPPER[6]	16	VCCPWRN_UPPER[15]
8	VCCPWRN_UPPER[7]	17	VCCPWRN_UPPER[16]
9	VCCPWRN_UPPER[8]	18	VCCPWRN_UPPER[17]

DMI: 125*4 = 500
 USB3.1: 125*5 = 625
 PCIe Gen1: 148*8 = 1184
 SATA3.1: 125*1 = 125
 PCIe Gen2: 123*2 = 246
 Total = 2620

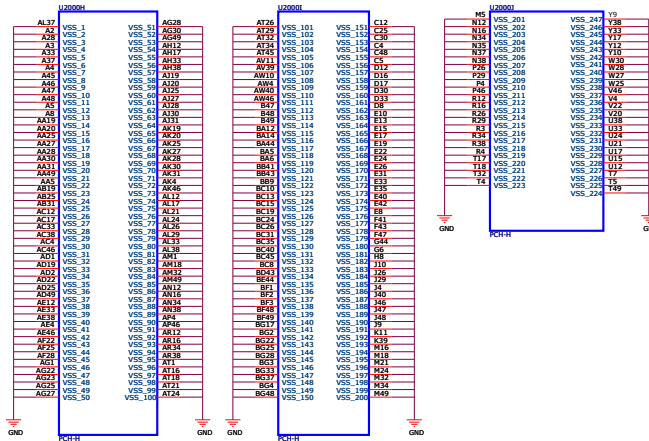
- +VCCPWRN_UPPER[0] = VCCPWRN_UPPER[0]
- +VCCPWRN_UPPER[1] = VCCPWRN_UPPER[1]
- +VCCPWRN_UPPER[2] = VCCPWRN_UPPER[2]
- +VCCPWRN_UPPER[3] = VCCPWRN_UPPER[3]
- +VCCPWRN_UPPER[4] = VCCPWRN_UPPER[4]
- +VCCPWRN_UPPER[5] = VCCPWRN_UPPER[5]
- +VCCPWRN_UPPER[6] = VCCPWRN_UPPER[6]
- +VCCPWRN_UPPER[7] = VCCPWRN_UPPER[7]
- +VCCPWRN_UPPER[8] = VCCPWRN_UPPER[8]
- +VCCPWRN_UPPER[9] = VCCPWRN_UPPER[9]
- +VCCPWRN_UPPER[10] = VCCPWRN_UPPER[10]
- +VCCPWRN_UPPER[11] = VCCPWRN_UPPER[11]
- +VCCPWRN_UPPER[12] = VCCPWRN_UPPER[12]
- +VCCPWRN_UPPER[13] = VCCPWRN_UPPER[13]
- +VCCPWRN_UPPER[14] = VCCPWRN_UPPER[14]
- +VCCPWRN_UPPER[15] = VCCPWRN_UPPER[15]
- +VCCPWRN_UPPER[16] = VCCPWRN_UPPER[16]
- +VCCPWRN_UPPER[17] = VCCPWRN_UPPER[17]

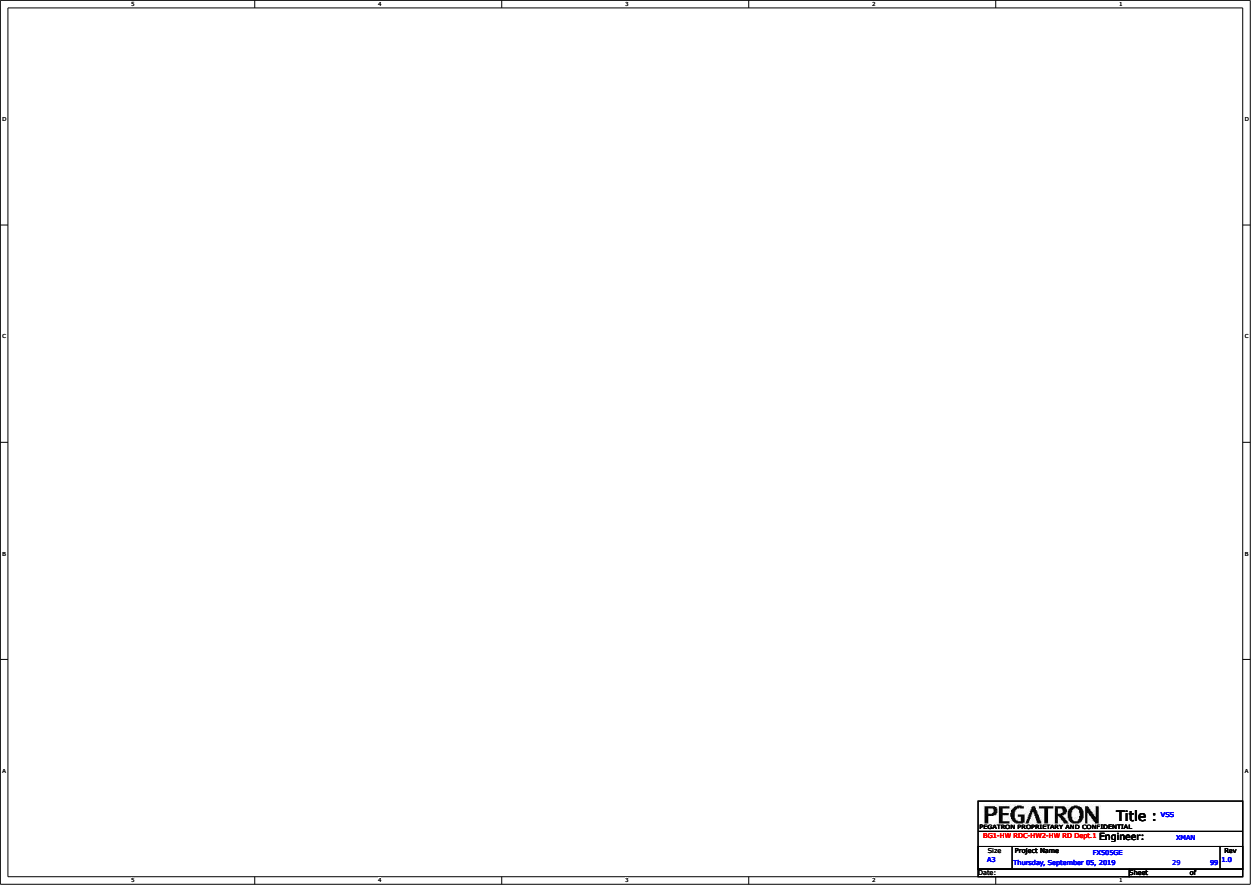


FX505 RF reserve @20180131

Close pin BB7 and AY8

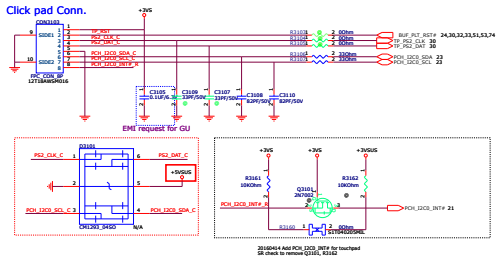
+3VSUS_ORG/+1.8VSUS to +1.0VSUS >200us (PCH06)



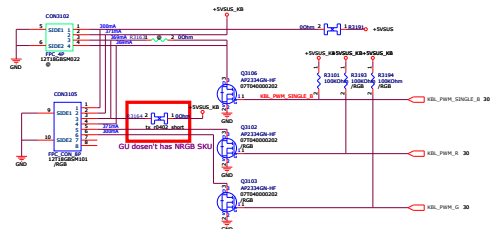


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PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dupr.1				
Engineer:			JOMAN	
Size	Project Name	FXSD5GSE	29	Rev
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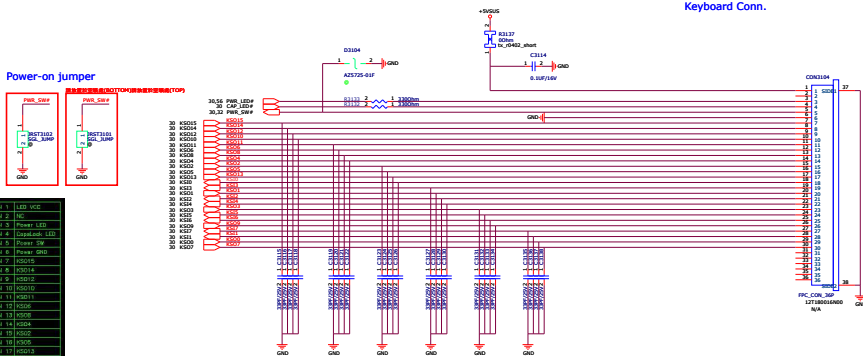
Click pad Conn.



KB Backlight Conn.

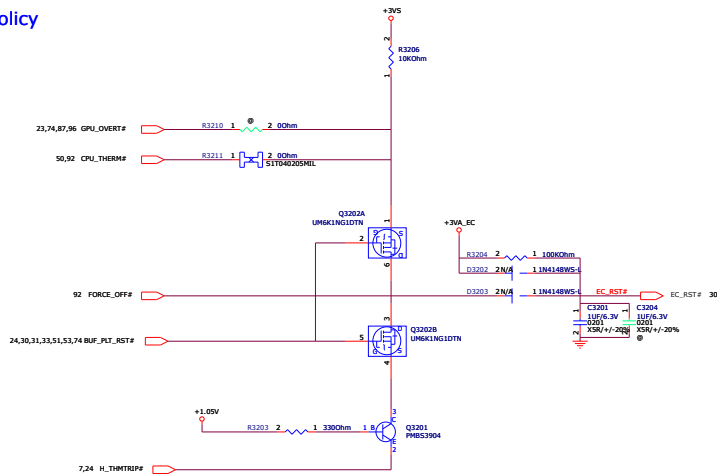


Keyboard Conn.



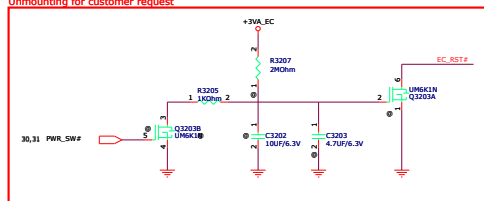
Pin 1	LED VCC
Pin 2	NC
Pin 3	Power LED
Pin 4	Power, LED
Pin 5	Power SW
Pin 6	Power GND
Pin 7	GPIO15
Pin 8	GPIO14
Pin 9	GPIO12
Pin 10	GPIO11
Pin 11	GPIO11
Pin 12	GPIO6
Pin 13	GPIO8
Pin 14	GPIO4
Pin 15	GPIO2
Pin 16	GPIO3
Pin 17	GPIO13
Pin 18	GPIO5
Pin 19	GPIO3
Pin 20	GPIO4
Pin 21	GPIO2
Pin 22	GPIO4
Pin 23	GPIO3
Pin 24	GPIO3
Pin 25	GPIO3
Pin 26	GPIO3
Pin 27	GPIO3
Pin 28	GPIO1
Pin 29	GPIO0
Pin 30	GPIO7
Pin 31	NC
Pin 32	NC
Pin 33	NC
Pin 34	NC
Pin 35	NC
Pin 36	NC

Thermal Policy

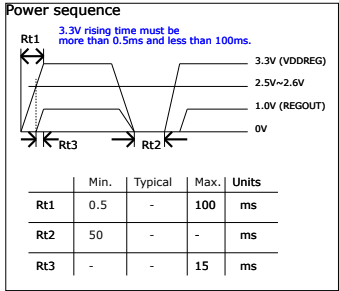
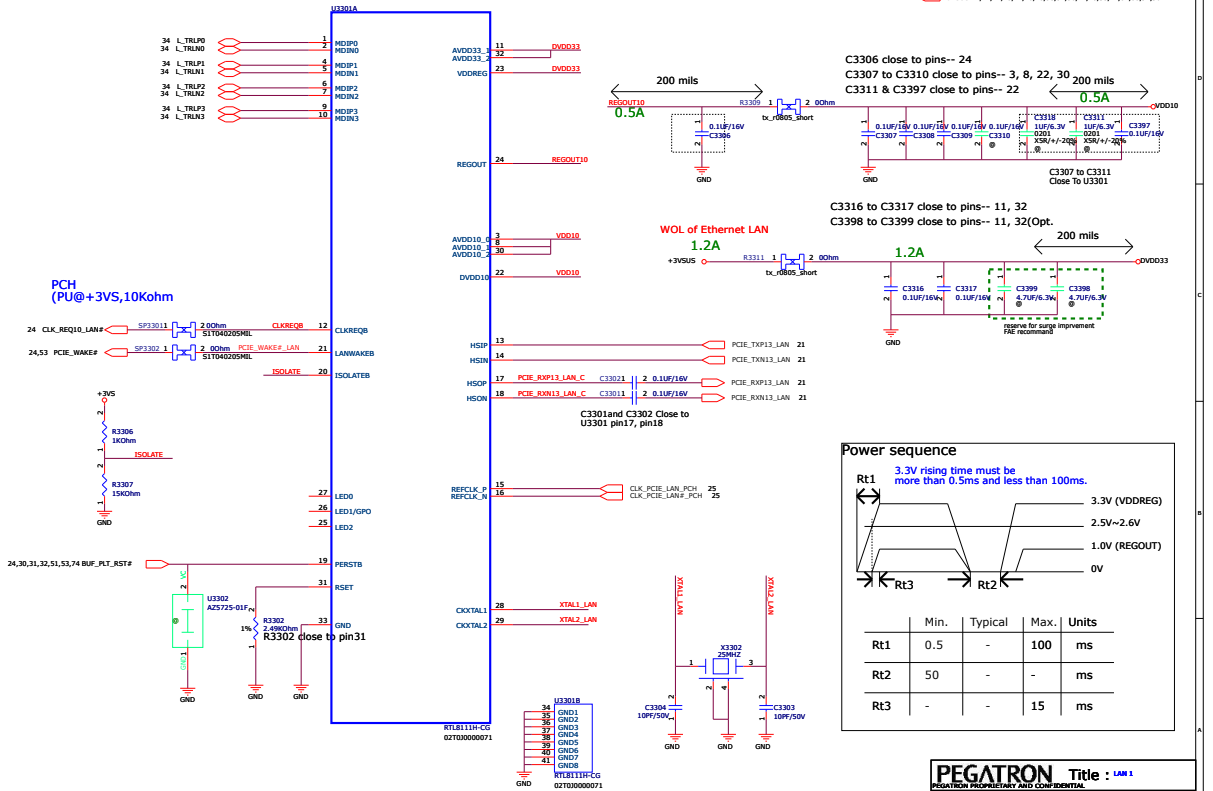


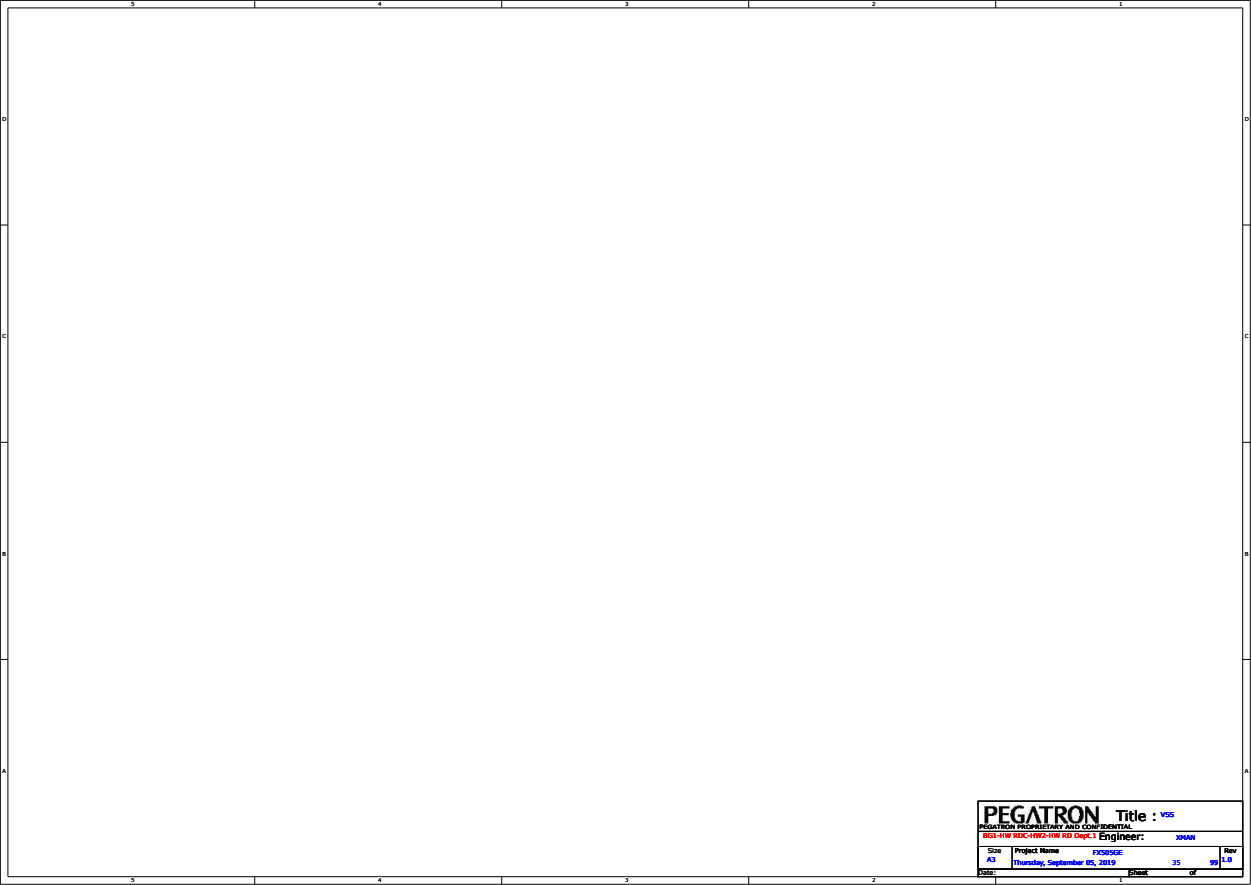
EC reset

Unmounting for customer request



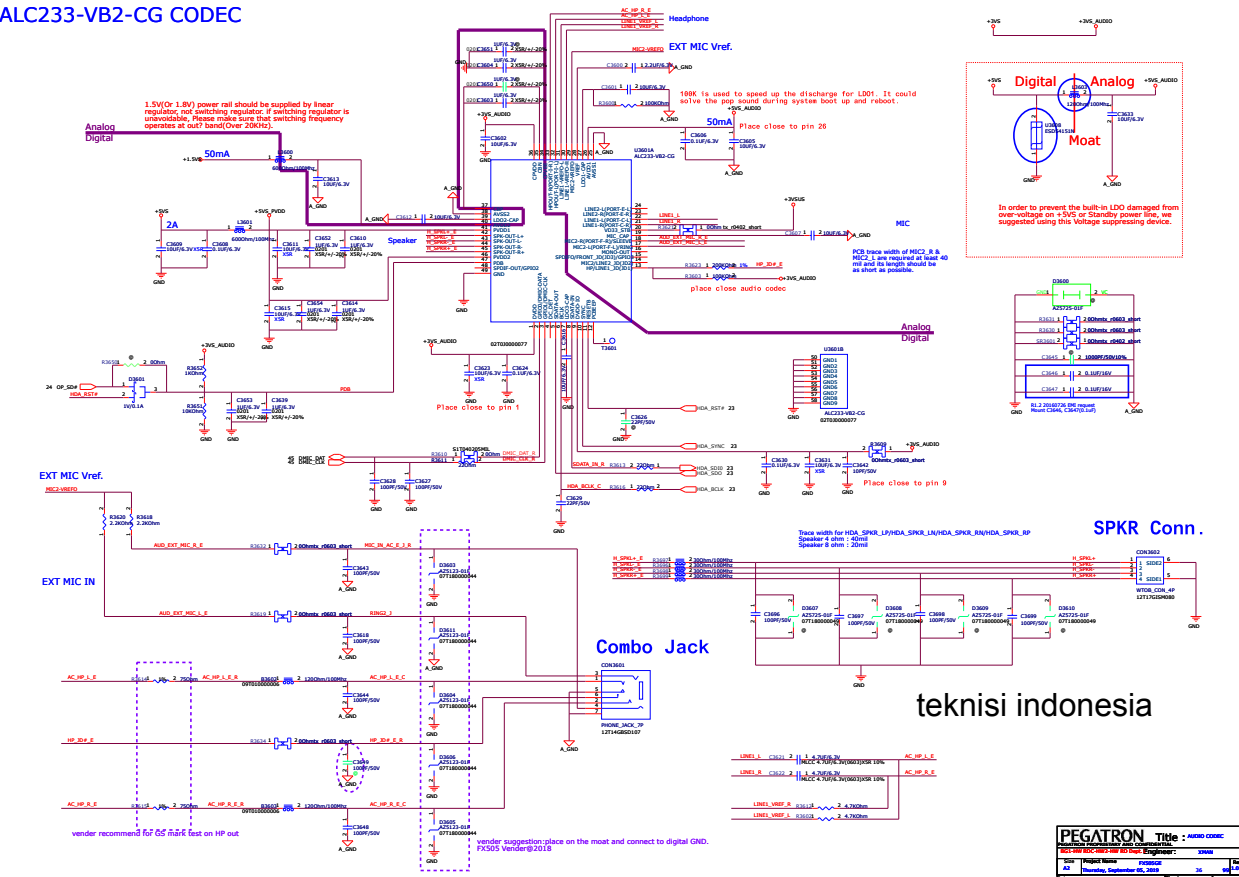
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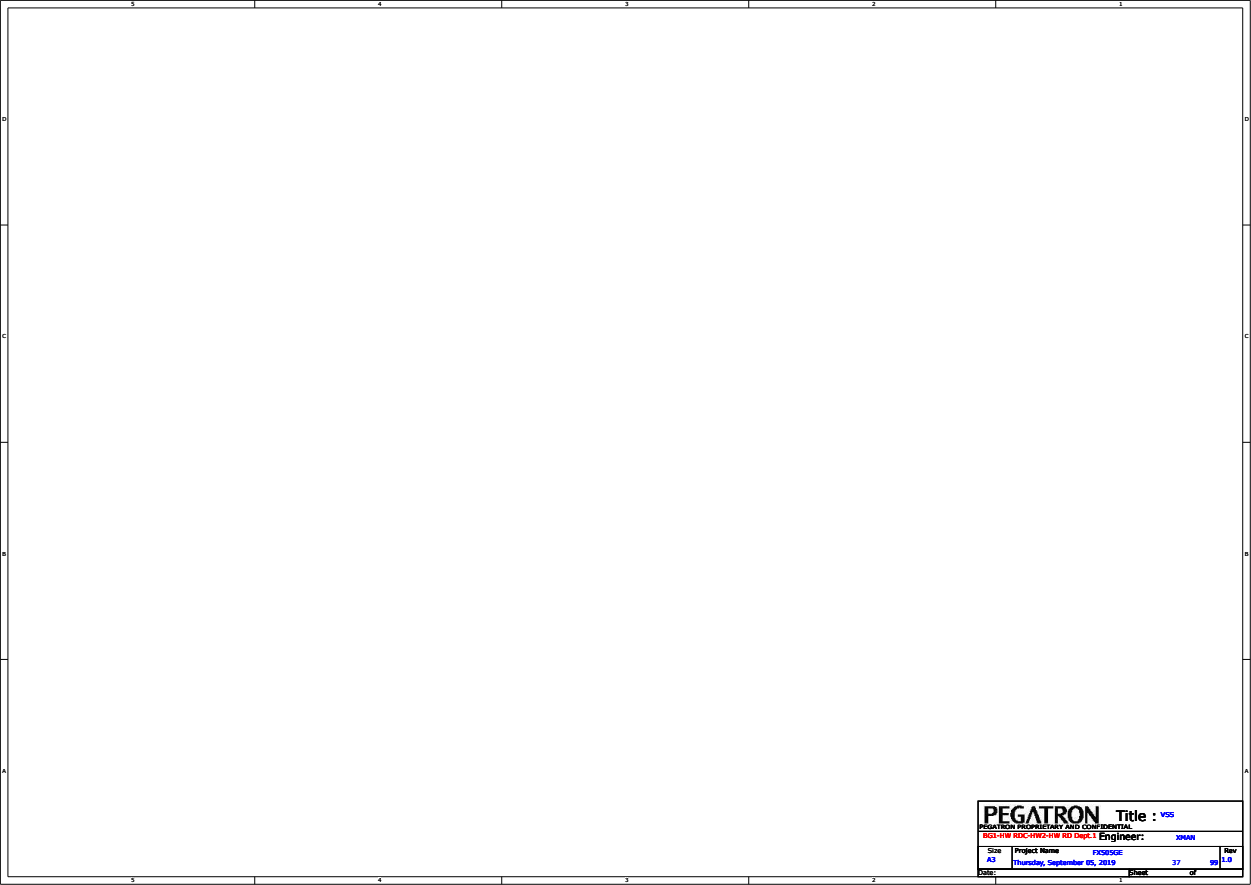




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BG3-HW RDC-HW2-HW RD Dupr.1 Engineer: XINXIN				
Size	Project Name	FXSD5DGE		Rev
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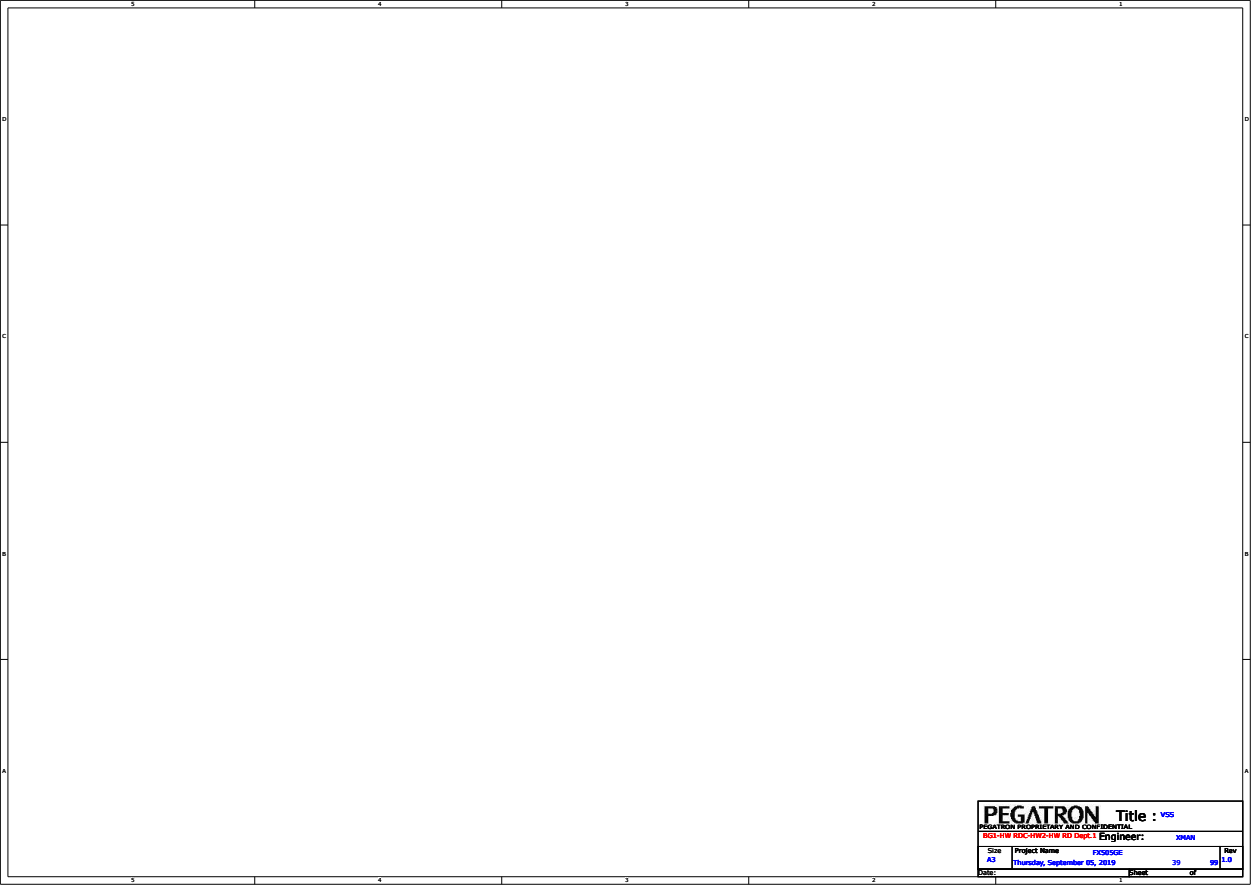
ALC233-VB2-CG CODEC



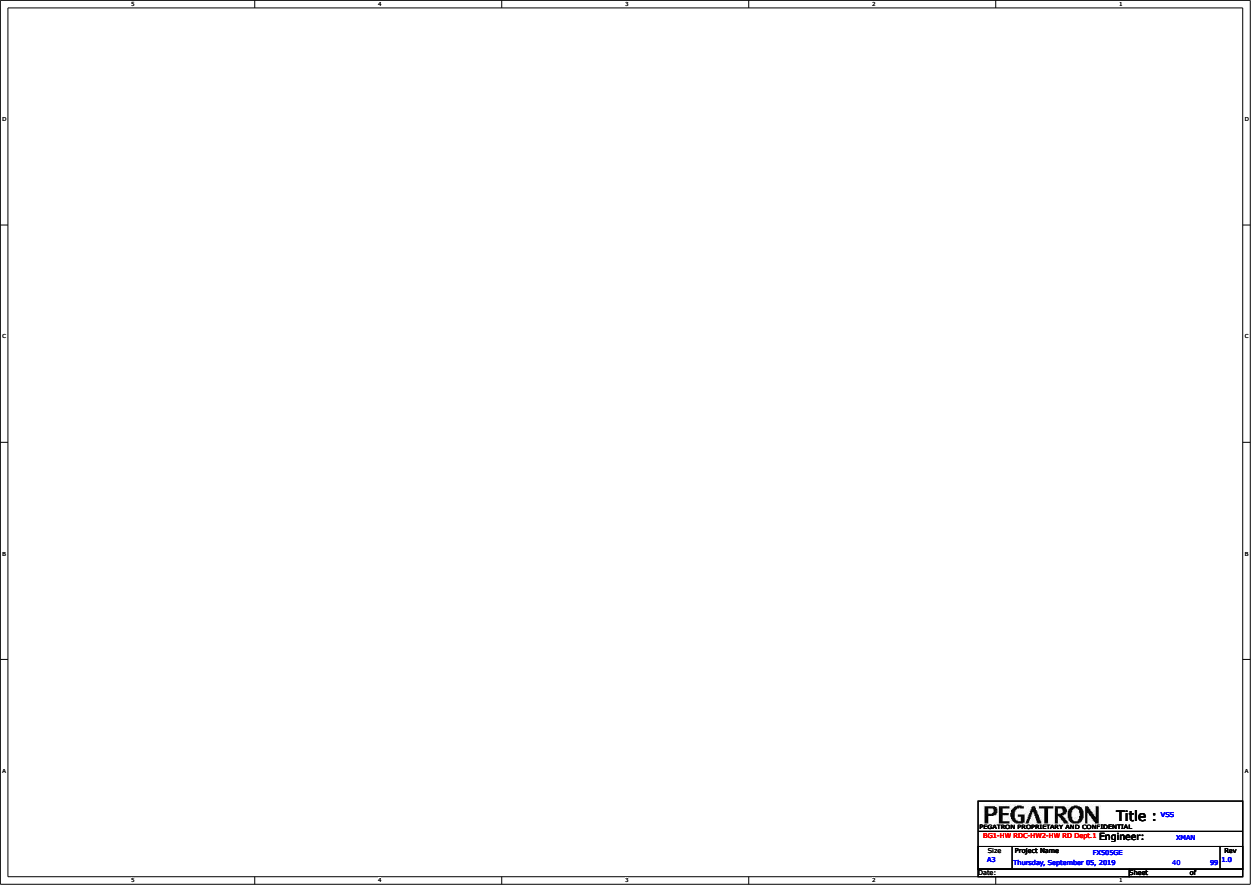


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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG3-HW RDC-HW2-HW RD Dupr.1 306AN			
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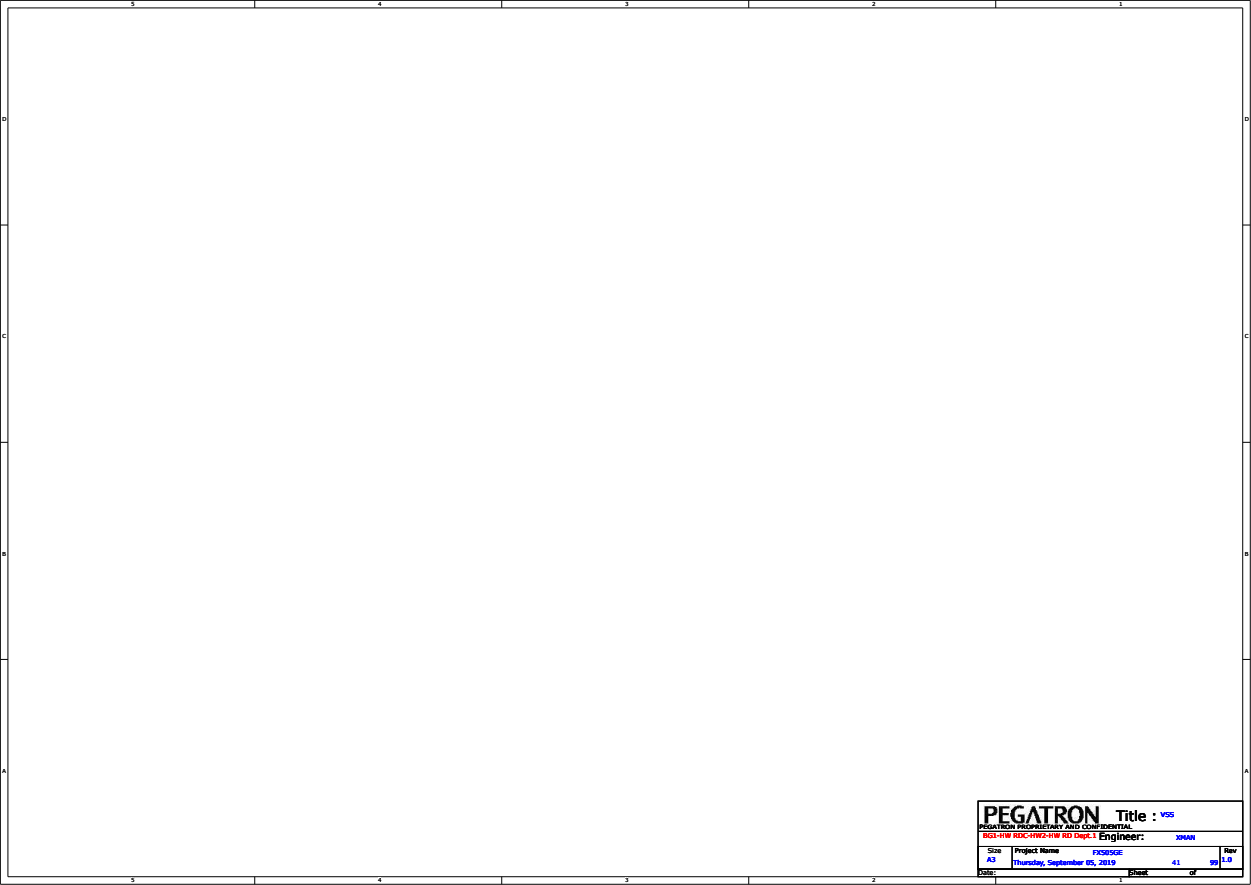




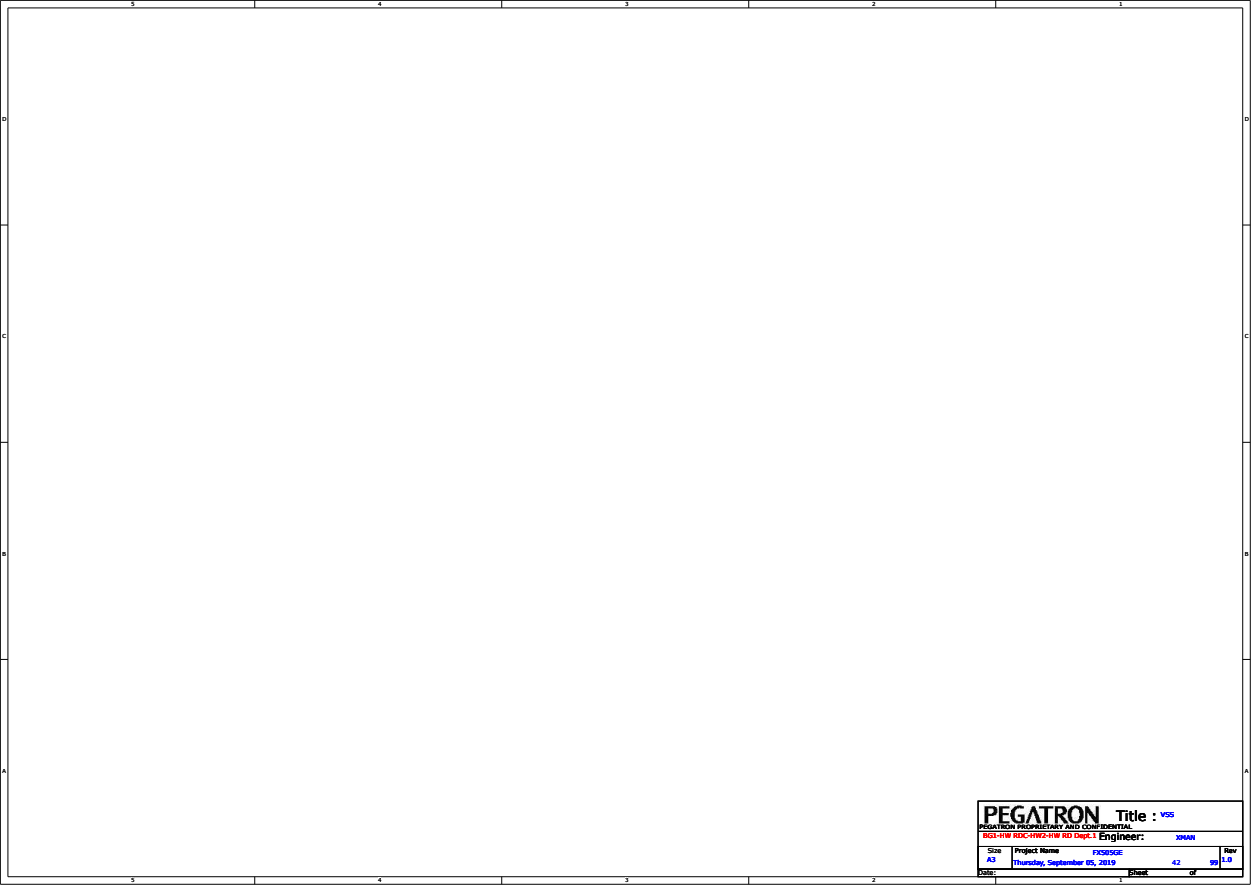
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BG3-HW RDC-HW2-HW RD Dupr.1 30MAN				
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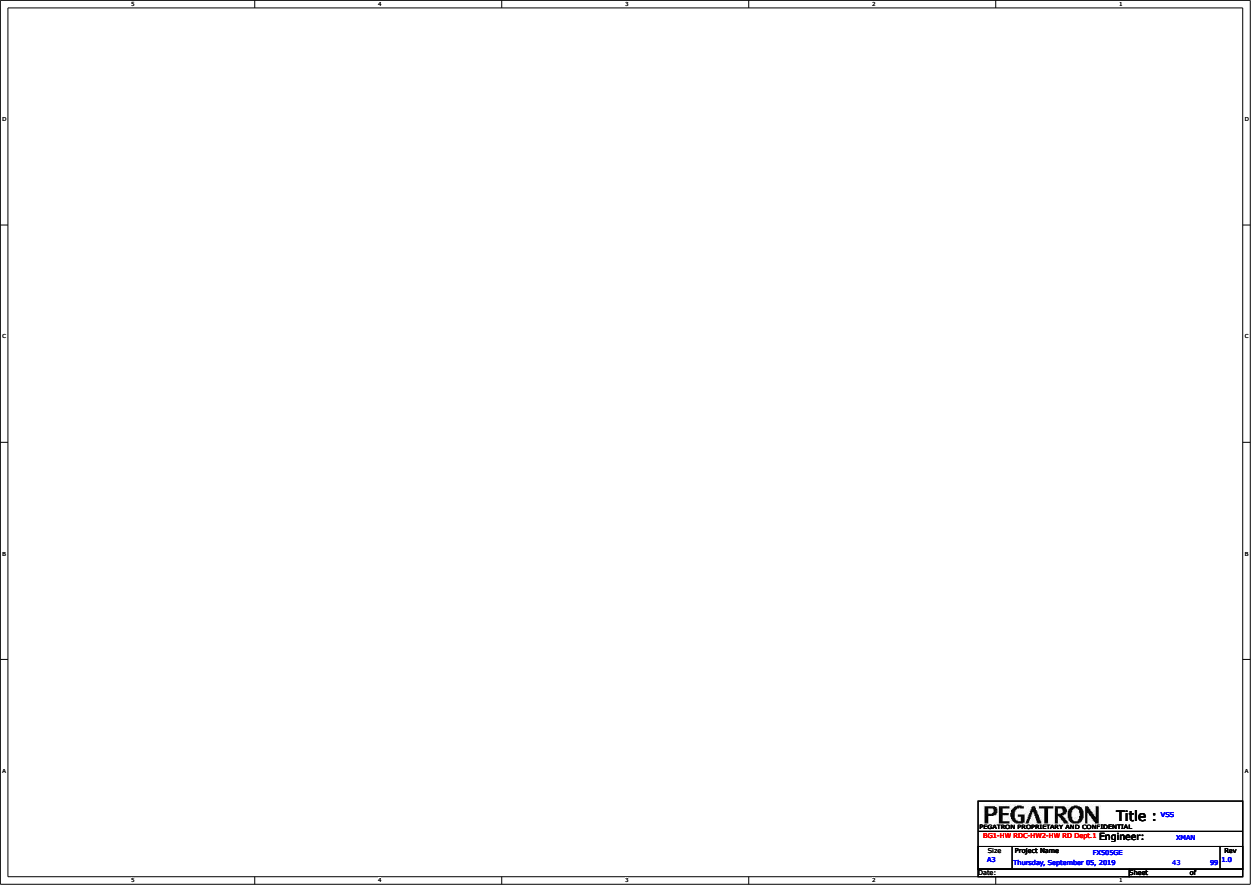
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PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dwg.1 JOHAN				
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PEGATRON Title : VSS				
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BG3-HW RDC-HW2-HW RD Dupr.1 J004N				
Size	Project Name	FXSD5GE	Rev	
A3	Thursday, September 05, 2019	41	99	1.0
DATE		Sheet 1 of 99		

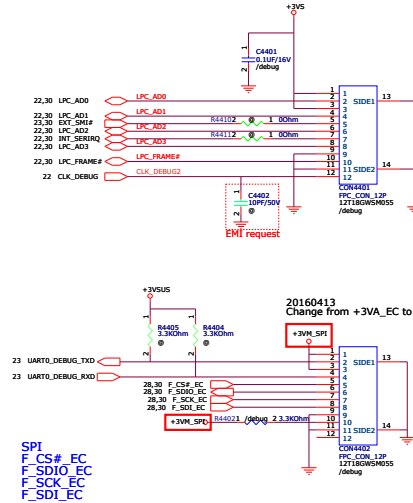


PEGATRON Title : VSS				
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dwg.1				
Engineer:			JOMAN	
Size	Project Name	FXSD5GSE		Rev
A3	Thursday, September 05, 2019	42	99	1.0
DATE		Sheet	of	
		1		

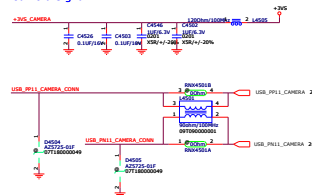


PEGATRON Title : VSS				
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dupr.1				
Engineer:			JOMAN	
Size	Project Name	FXSD5GSE		Rev
A3	Thursday, September 05, 2019	43	99	1.0
DATE		Sheet	of	
		1		

+3VS  +3VS 7,17,21,22,23,24,28,30,31,32,33,36,45,48,50,51,57,74,87,88,89,91,92,96
 +3VSUS  +3VSUS 7,21,22,23,24,26,28,30,31,33,36,48,53,74,81,88,92,96
 +3VM_SPI  +3VM_SPI 28

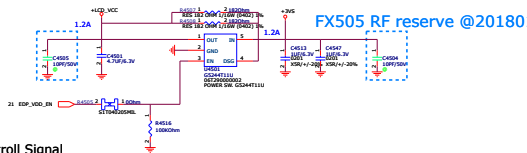
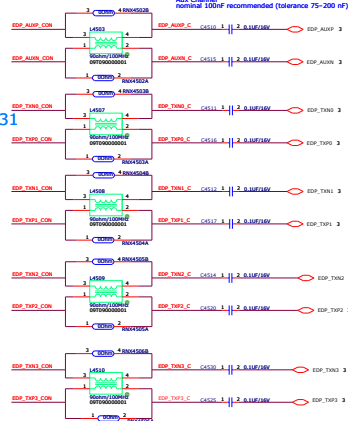


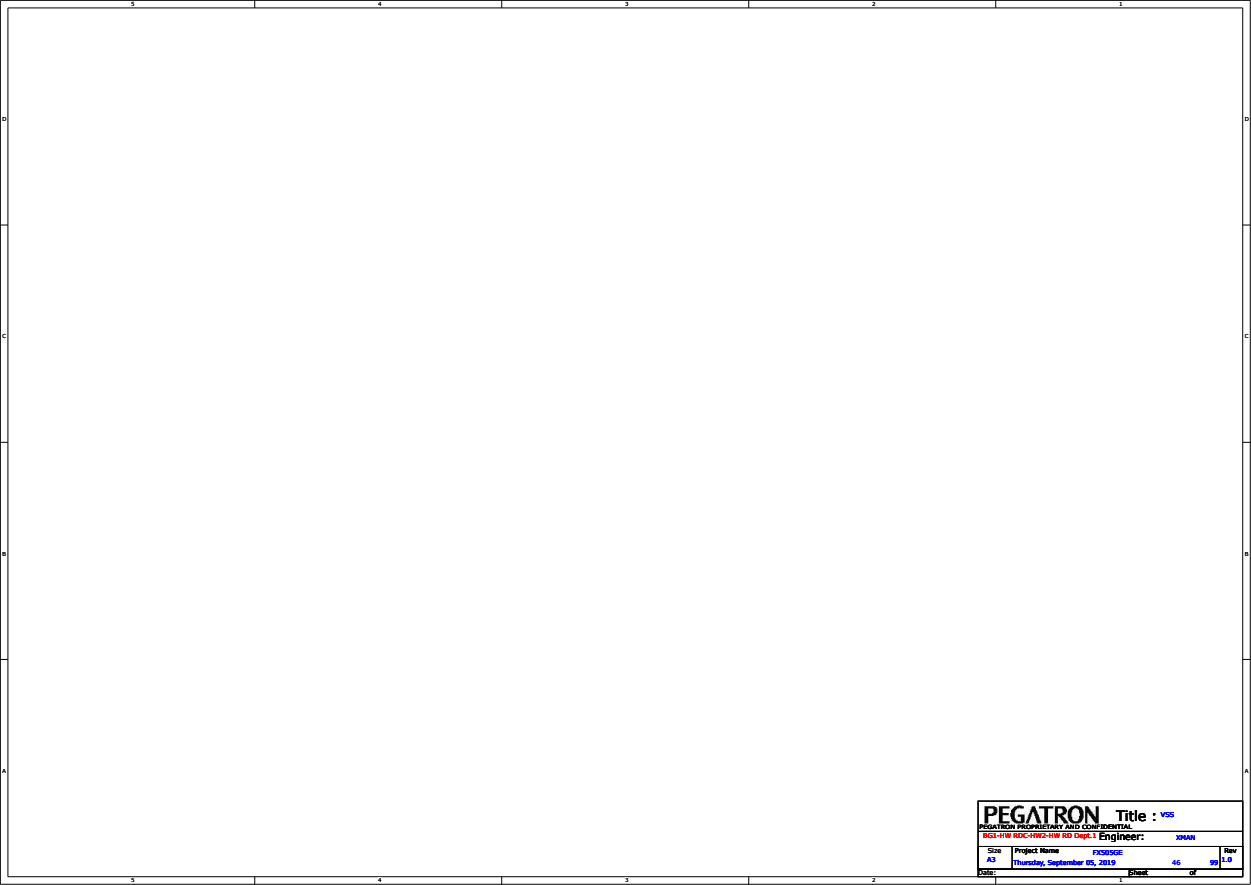
+SYS_CAMERA



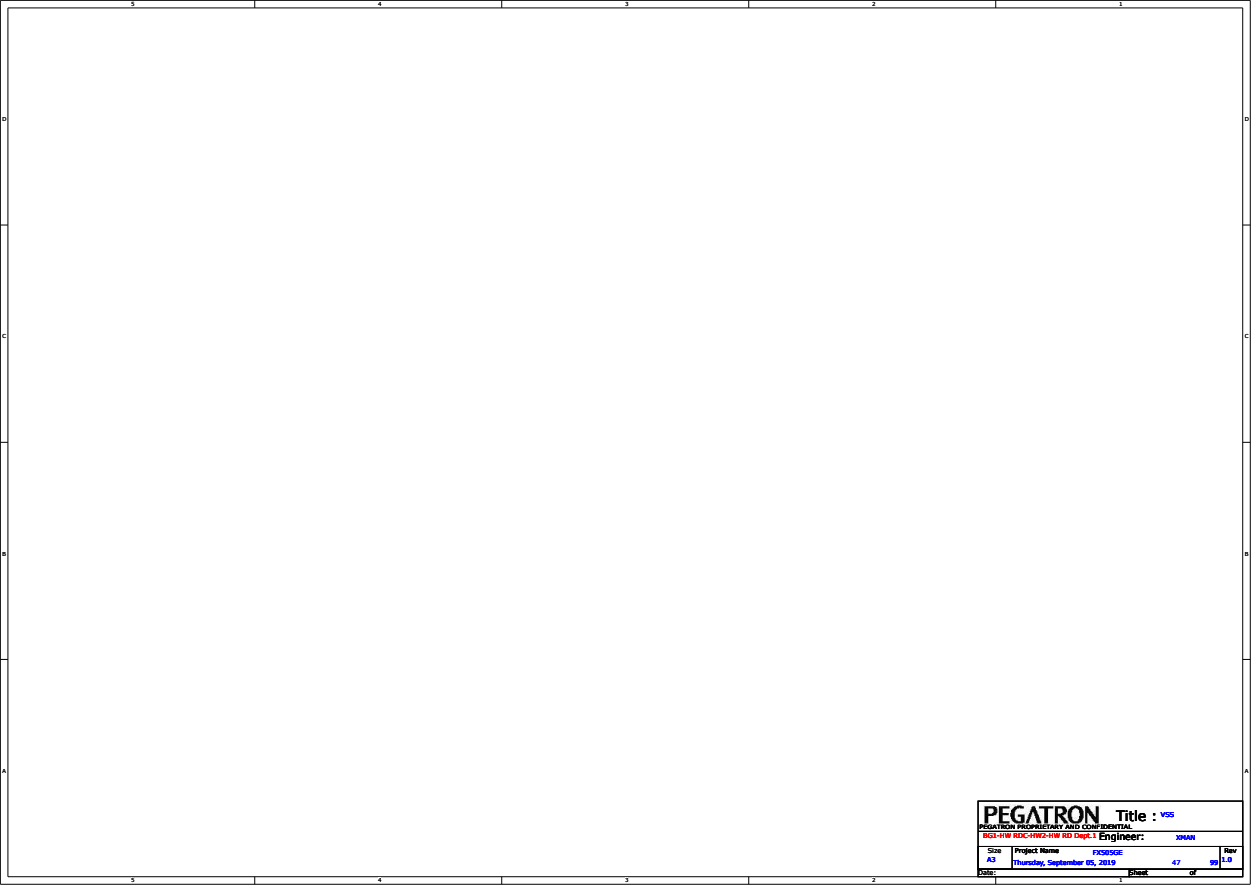
CFL PDG:
AC caps are required to be placed before the motherboard eDP* connector
Main Link
nominal 100nF recommended (tolerance 75~265 nF)
Aux Channel
nominal 100nF recommended (tolerance 75~200 nF)

FX505 RF reserve @20180131

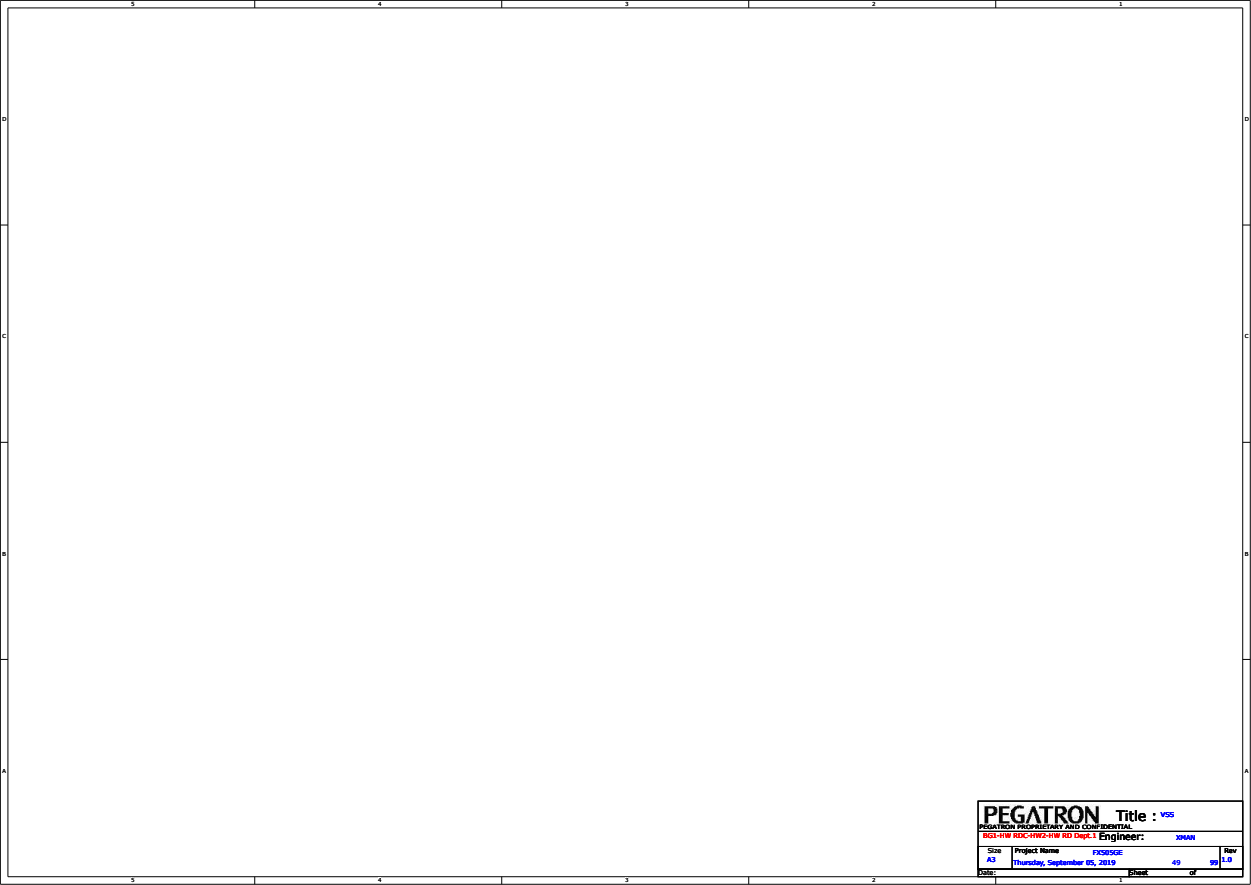
[illegible]



PEGATRON Title : VSS			
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG3-HW RDC-HW2-HW RD Dwg.1 J004N			
Size	Project Name	FXSDSGE	Rev
A3	Thursday, September 05, 2019	46	99 1.0
DATE		Sheet of	



PEGATRON Title : VSS				
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dupr.1				
Engineer:			JOMAN	
Size	Project Name	FXSD5GSE	47	Rev
A3	Thursday, September 05, 2019		99	1.0
DATE		Sheet	of	
		1		

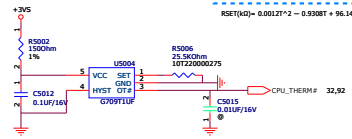


PEGATRON Title : VSS				
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dupr.1 Engineer: JOMAN				
Size	Project Name	FXSDSGE		Rev
A3	Thursday, September 05, 2019	49	99	1.0
DATE		Sheet	of	
		1		

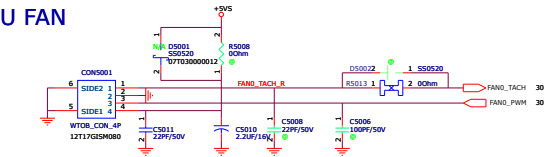
CPU Thermal Sensor

temperature set=85 C

$RSET(K\Omega) = 0.0012T + 2 - 0.9308T + 96.147$

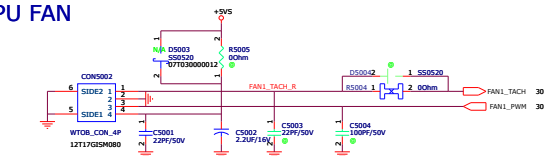


CPU FAN



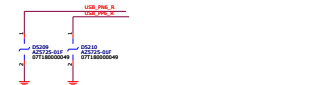
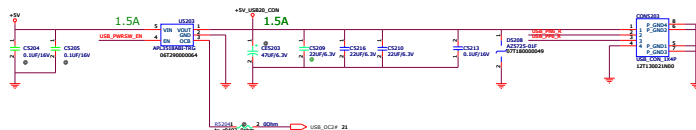
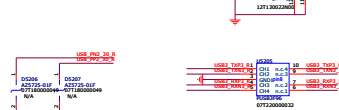
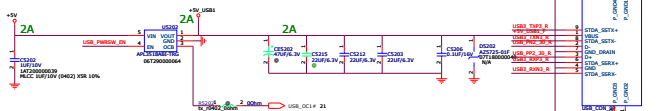
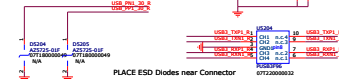
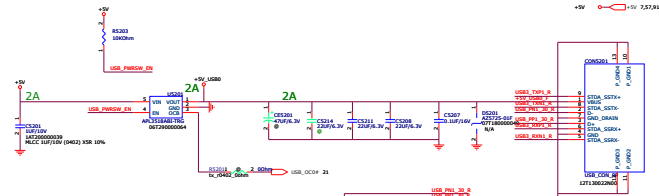
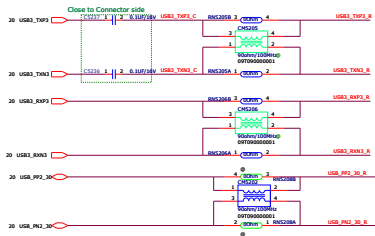
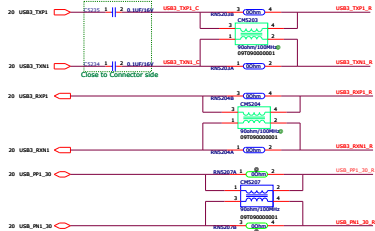
EC(PU@+3VS,10Kohm

GPU FAN



EC(PU@+3VS,10Kohm

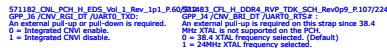
52.USB3.0



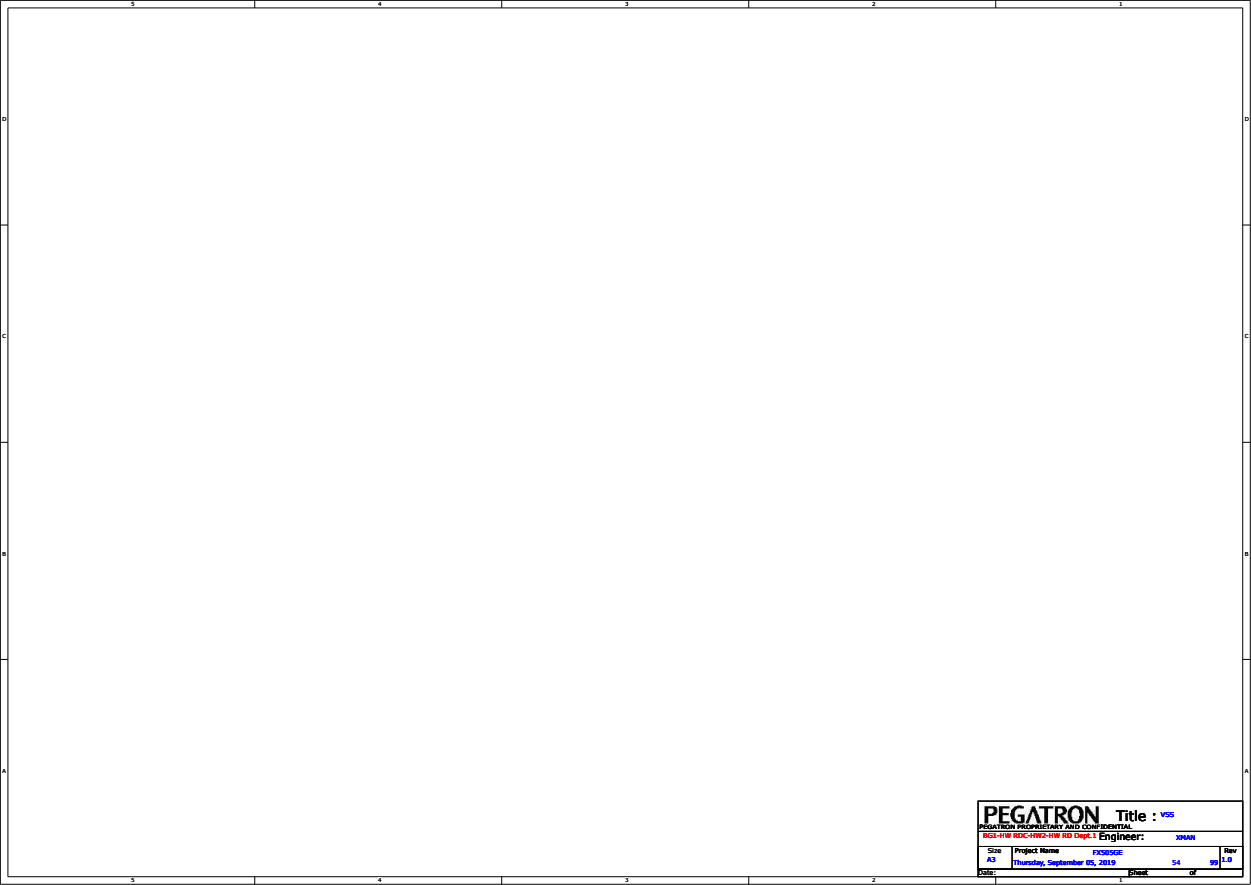
T

WLAN bypass capacitors:

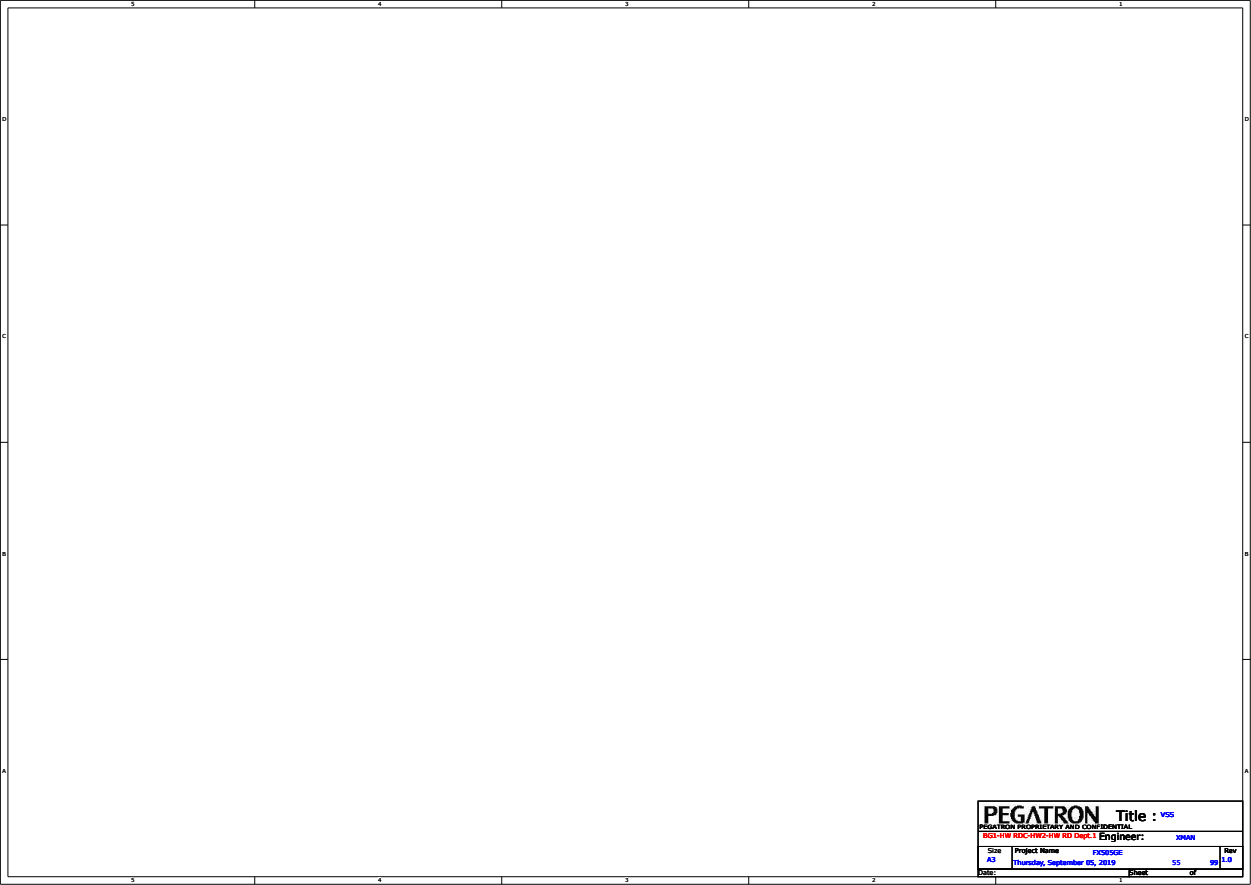
1 EA +2V2



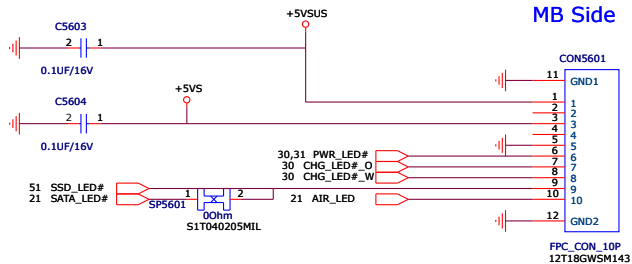
PEGATRON Title : WLAN
 POSITION PROPRIETARY AND CONFIDENTIAL
 BCL-HW RDC-HW2-HW RD Dept. Engineer: XMM
 Size Project Name FCS05GE
 A2 Thursday, September 05, 2019 5:3 9



PEGATRON Title : VSS				
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dupr.1				
Engineer:			JOMAN	
Size	Project Name	FXSD5GSE		Rev
A3	Thursday, September 05, 2019	54	99	1.0
DATE		Sheet	of	
		1		



PEGATRON Title : VSS				
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dupr.1				
Engineer:			JOMAN	
Size	Project Name	FXSD5DGE		Rev
A3	Thursday, September 05, 2019	55	99	1.0
DATE		Sheet	of	
		1		



+5VSUS ○ +5VSUS 31,81
 +5VS ○ +5VS 36,48,50,51,57,80,87,89,91

Power LED

AIR PLANE LED

NOTE: AIR_LED#_R
 High -> airplane mode ON -> LED ON
 Low -> airplane mode OFF -> LED OFF

Charger LED

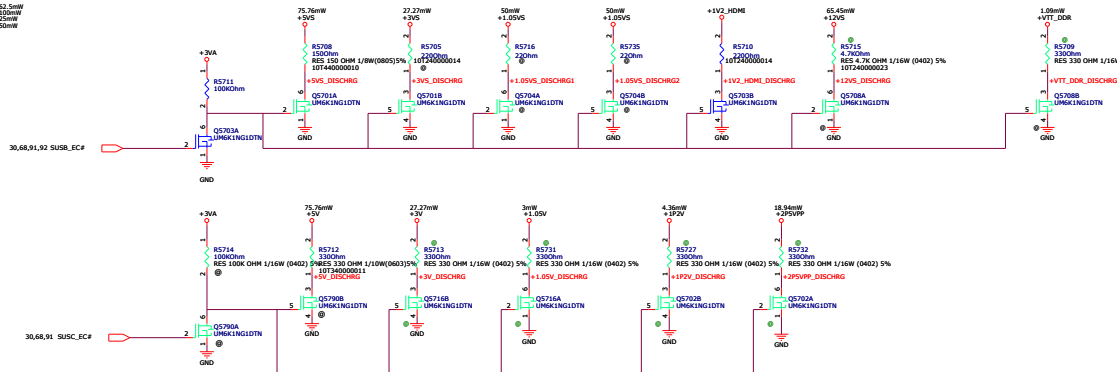
PCB/ID LOCATION

PWR LED LED5601 Charger LED LED5606 HDD LED LED5604 RF LED LED5602

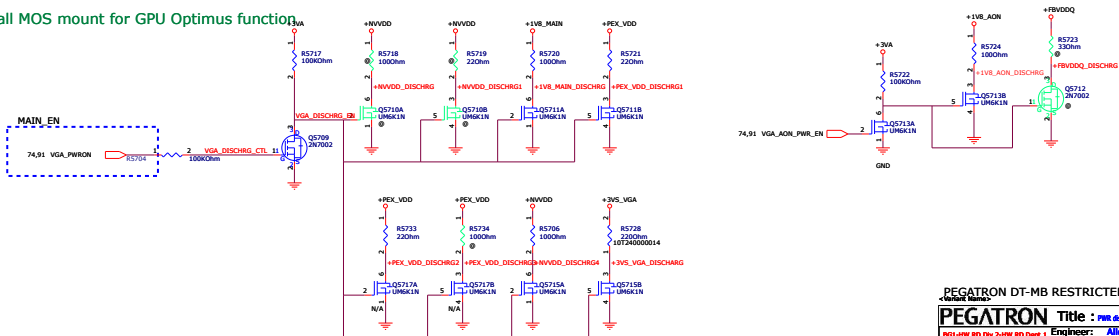
HDD LED

PEGATRON		Title : LED	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW RDC-HW2-HW RD Dept.		Engineer: XMAN	
Size A4	Project Name FX505GE	Rev 56	99
Date: Thursday, September 05, 2019	Sheet 1 of 1.0		

$V=2/R$
 $0402 = 1/16W = 63.5mW$
 $0603 = 1/10W = 100mW$
 $0805 = 1/8W = 125mW$
 $1206 = 1/4W = 250mW$

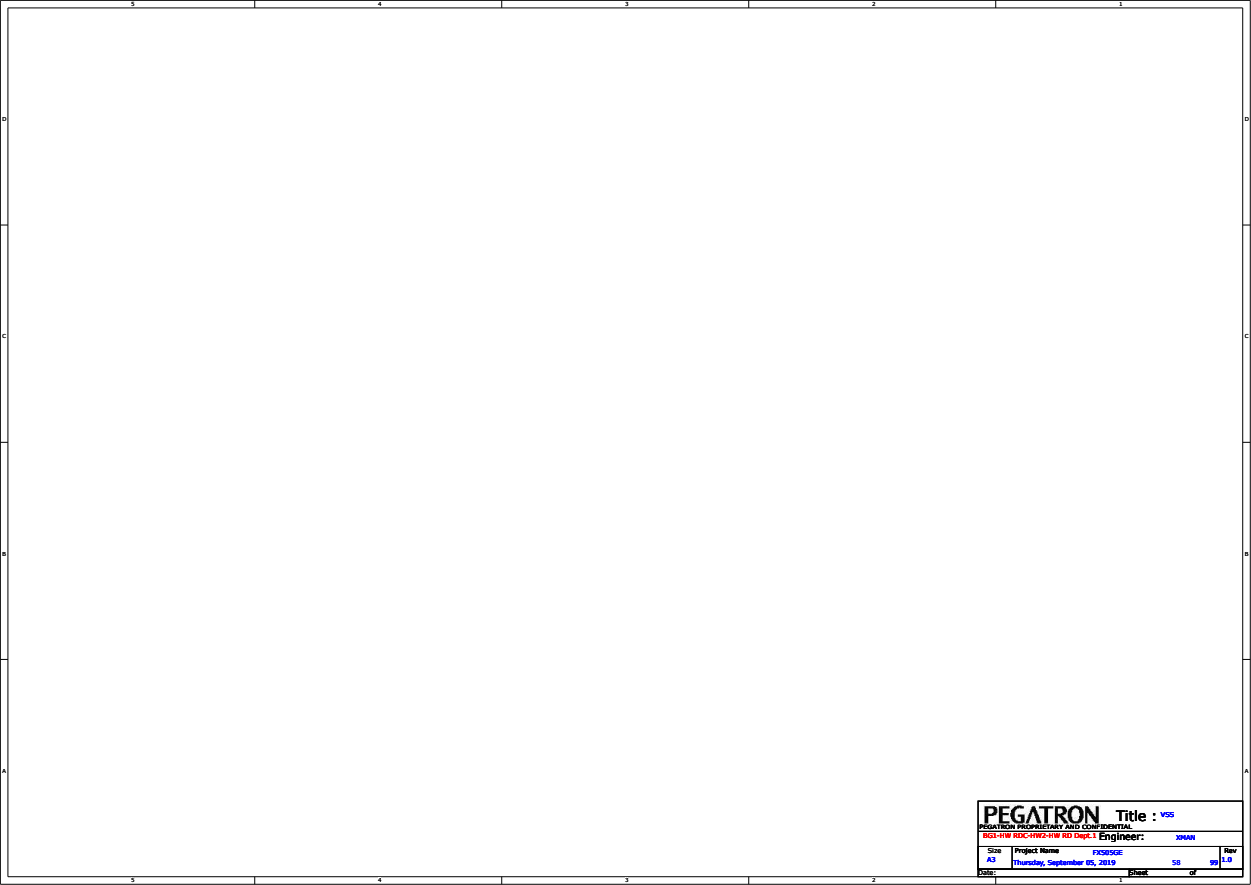


all MOS mount for GPU Optimus function

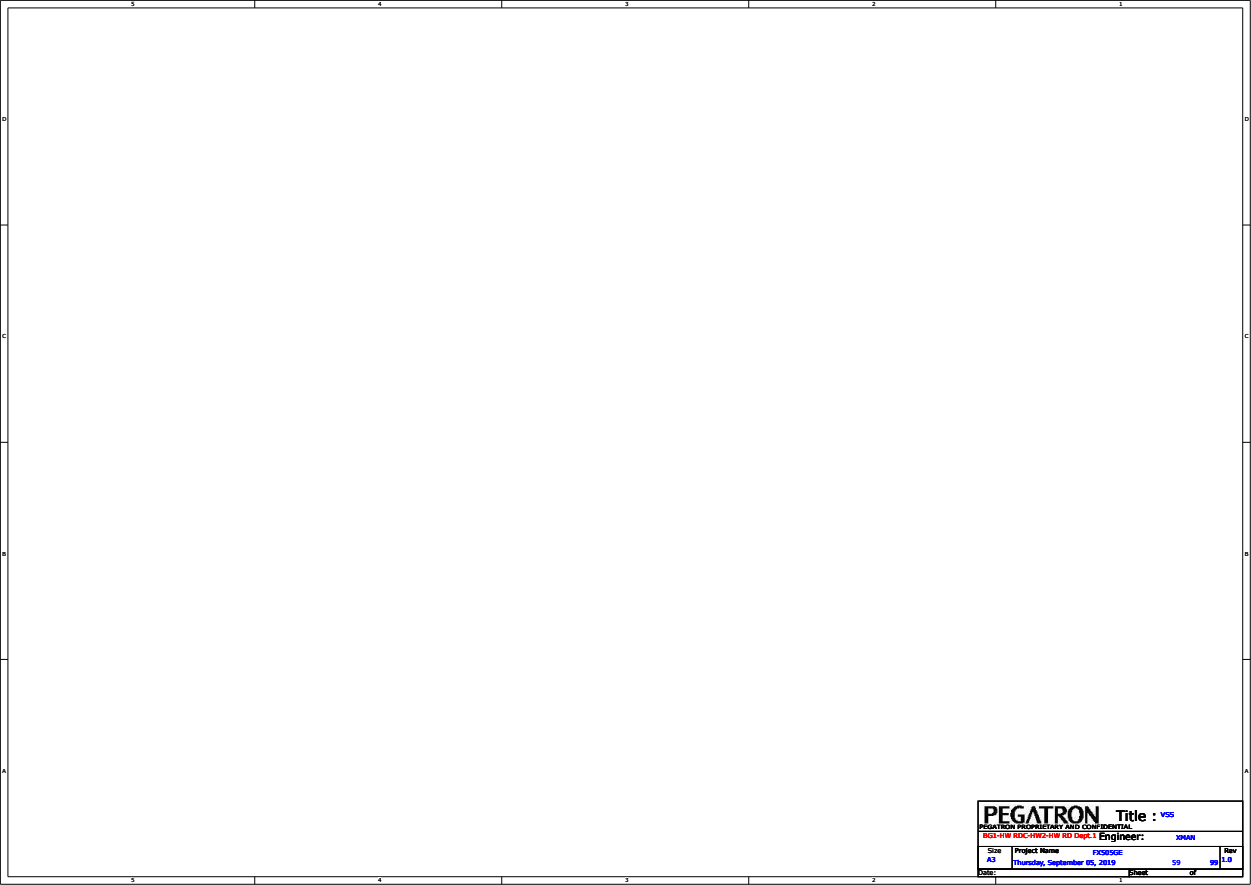


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : PWR discharge	
RGI-4W RD Div.2-HW RD Dept.1		Engineer: Allen Kuo	
Size	Project Name	Rev	
FX505GE		1.0	
Date: Thursday, September 04, 2014		Sheet: 57 of 90	

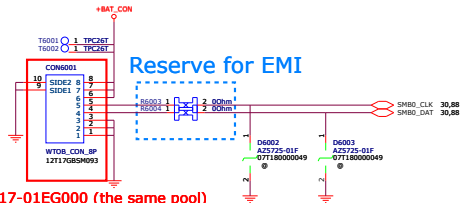


PEGATRON Title : VSS				
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dwg.1				
Engineer:			JOMAN	
Size	Project Name	FXSDSGE		Rev
A3	Thursday, September 05, 2019	SB	99	1.0
DATE		Sheet	of	
		1		



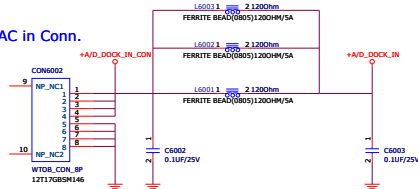
PEGATRON Title : VSS				
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dupr.1				
Engineer:			JOMAN	
Size	Project Name	FXSD5GSE		Rev
A3	Thursday, September 05, 2019	59	99	1.0
DATE		Sheet	of	
		1		

Battery Conn.

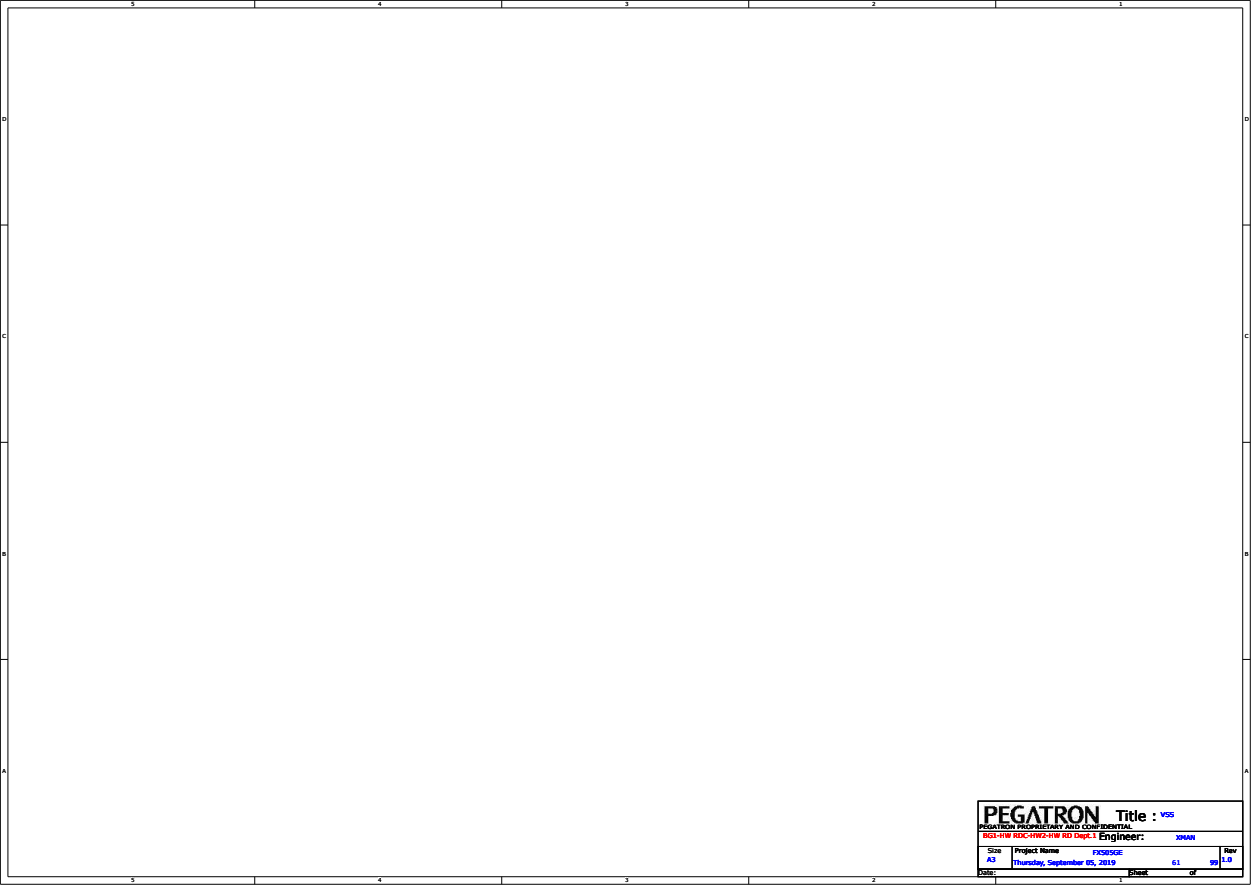


ABBA assign: 1217-017L000, doesn't include 1217-01EG000 (the same pool)

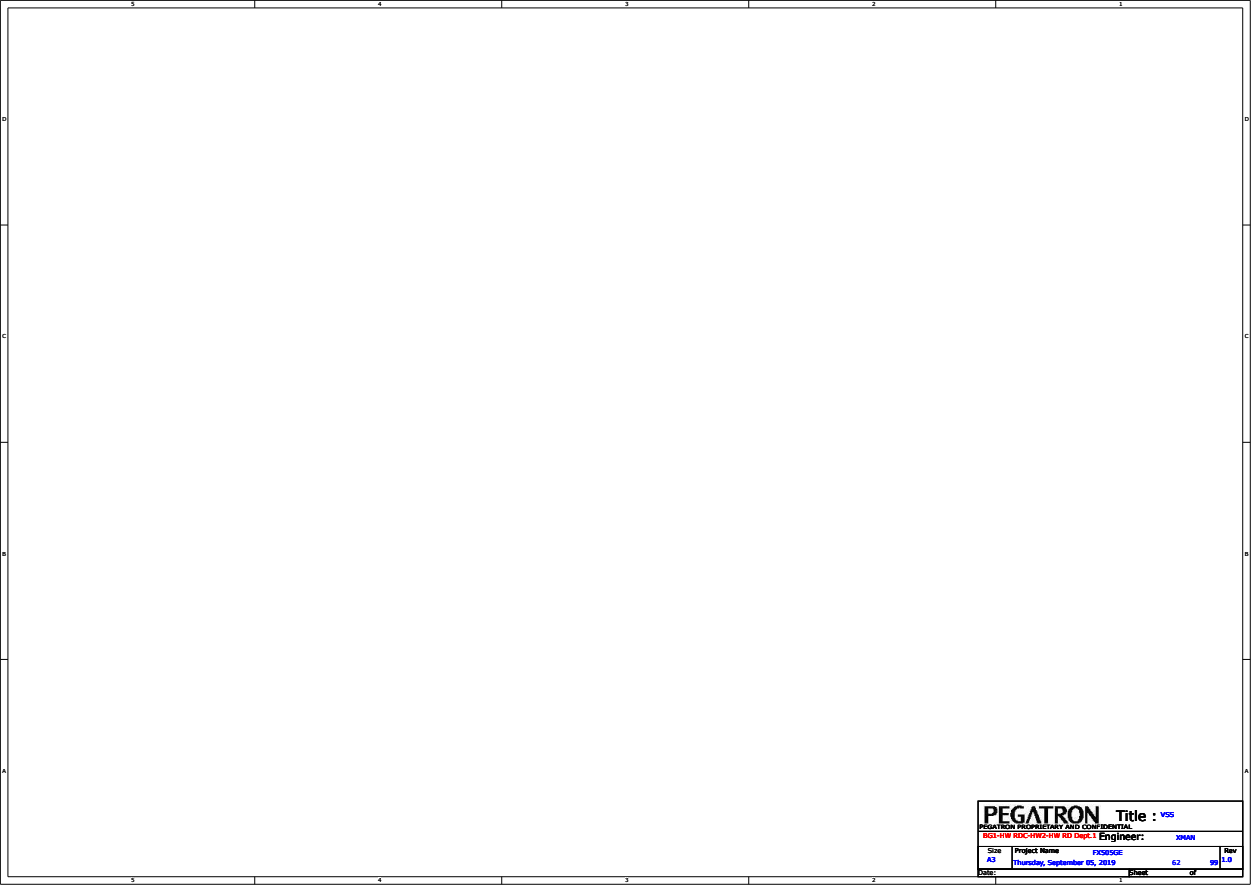
AC in Conn.



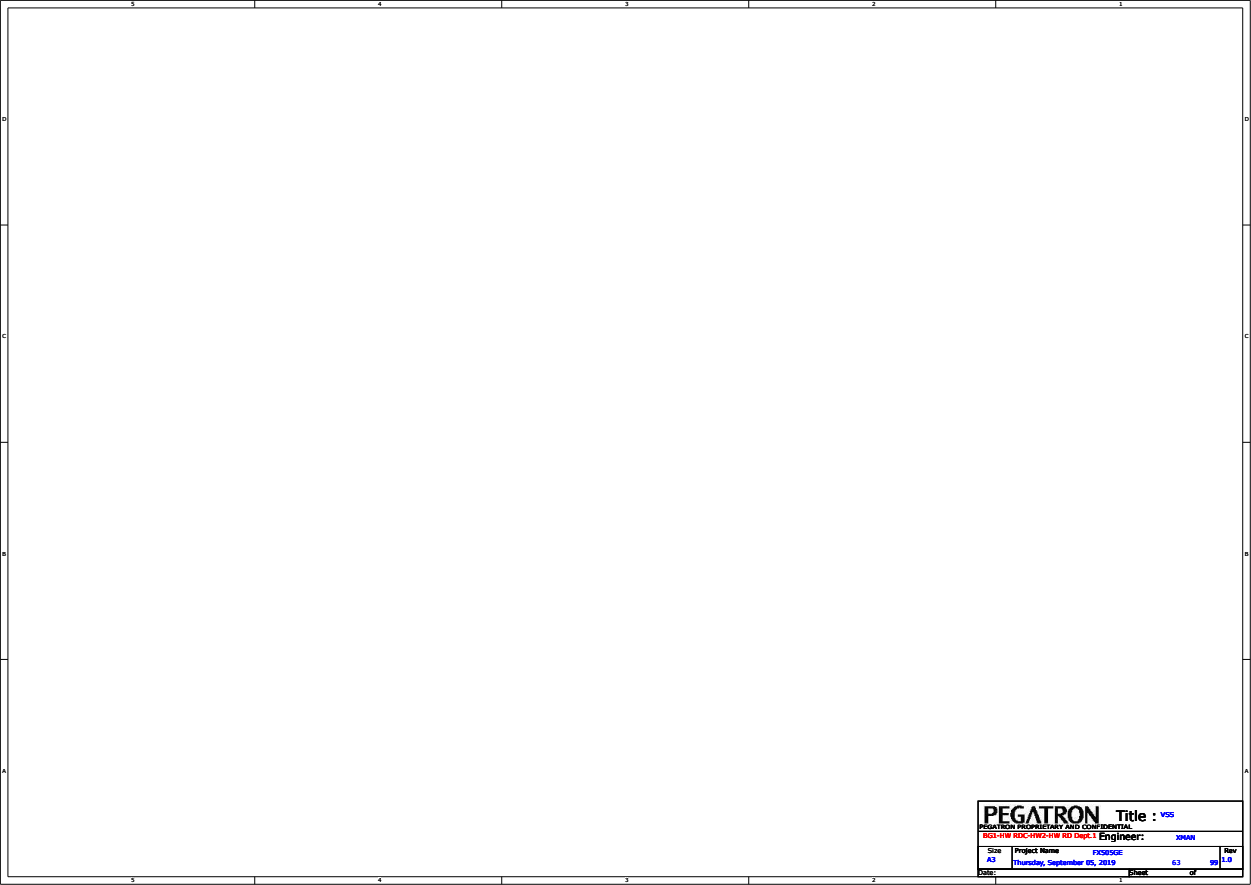
FX505GE N17P Adaptor: 120W
FX505GE N17E Adaptor: 150W



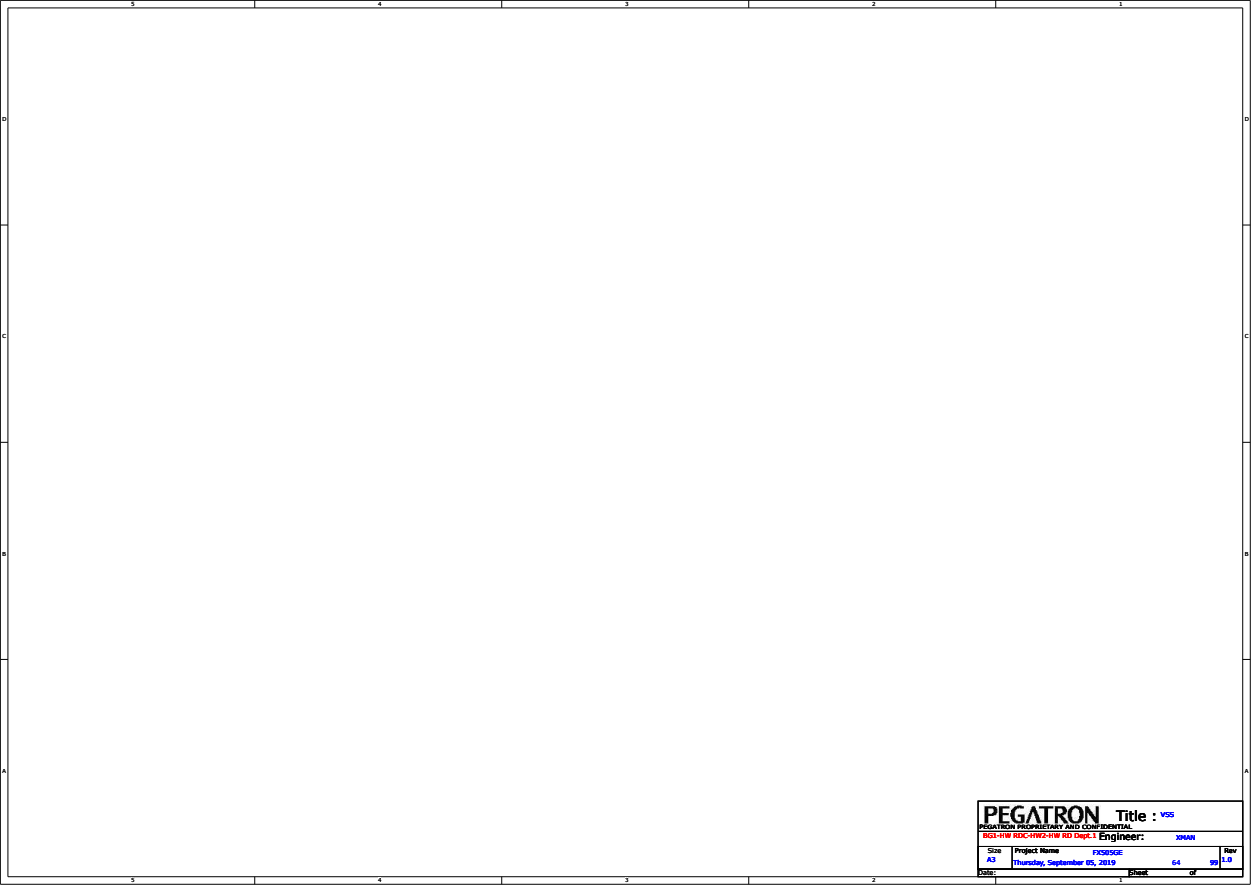
PEGATRON Title : VSS				
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dwg-1				
Engineer:			JOMAN	
Size	Project Name	FXSDSGE		Rev
A3	Thursday, September 05, 2019	6.1	99	1.0
DATE		Sheet	of	
		1		



PEGATRON Title : VSS				
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dupr.1 J004N				
Size	Project Name	FXSDSGE	Rev	
A3	Thursday, September 05, 2019	6.2	99	1.0
DATE		Sheet 1 of 99		

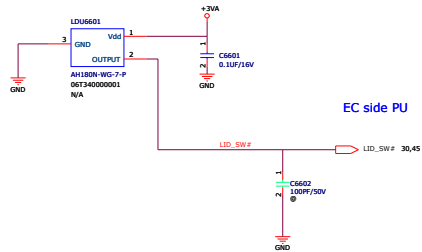


PEGATRON Title : VSS				
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dapt.1				
J004N				
Size	Project Name	FXSD5GE	Rev	
A3	Thursday, September 05, 2019	63	99	1.0
DATE		Sheet 1 of 99		

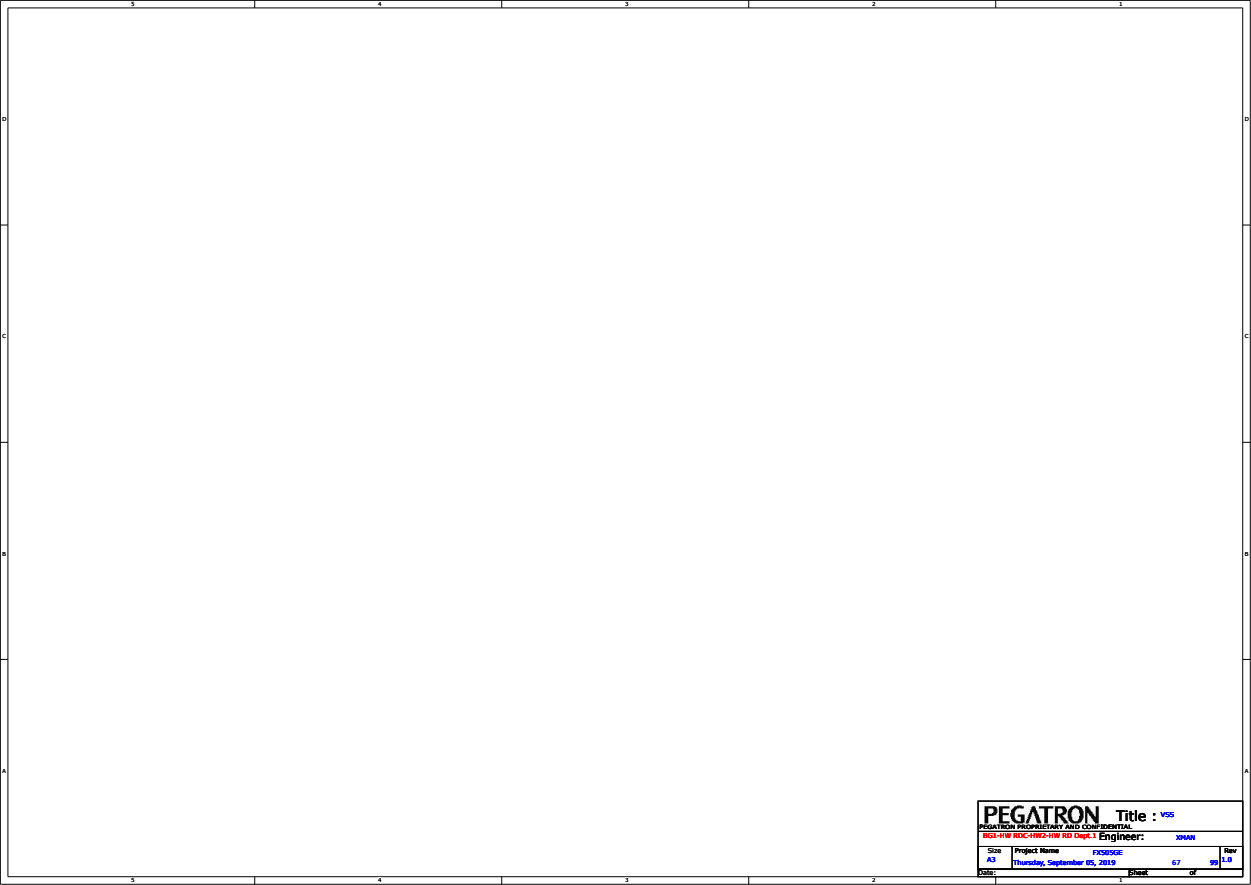


PEGATRON Title : VSS				
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dwg-1				
Engineer:			JOMAN	
Size	Project Name	FXSDSGE		Rev
A3	Thursday, September 05, 2019	64	99	1.0
DATE		Sheet	of	
		1		

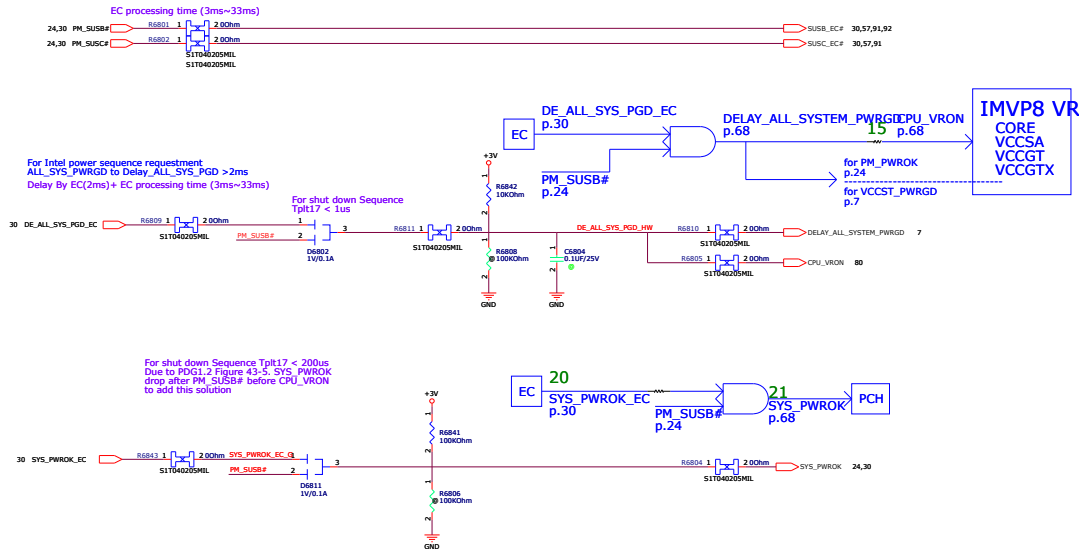
Hall sensor

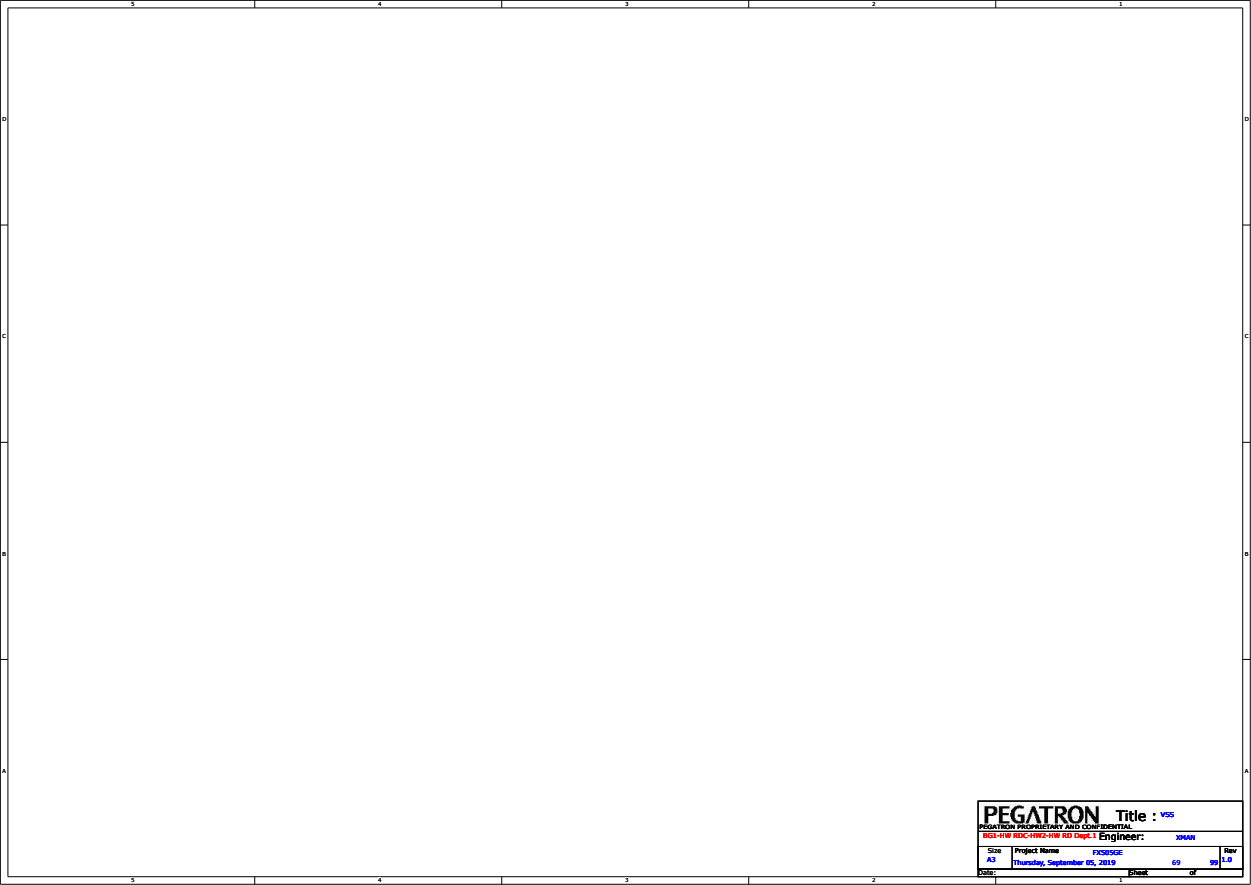


+3VA 25,30,57,74,81,88,93,97



PEGATRON Title : VSS			
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG3-HW RDC-HW2-HW RD Dwg-1			
Engineer:		JHANN	
Size	Project Name	FXSDSGE	Rev
A3	Thursday, September 05, 2019	67	99 1.0
DATE		Sheet	of
		1	



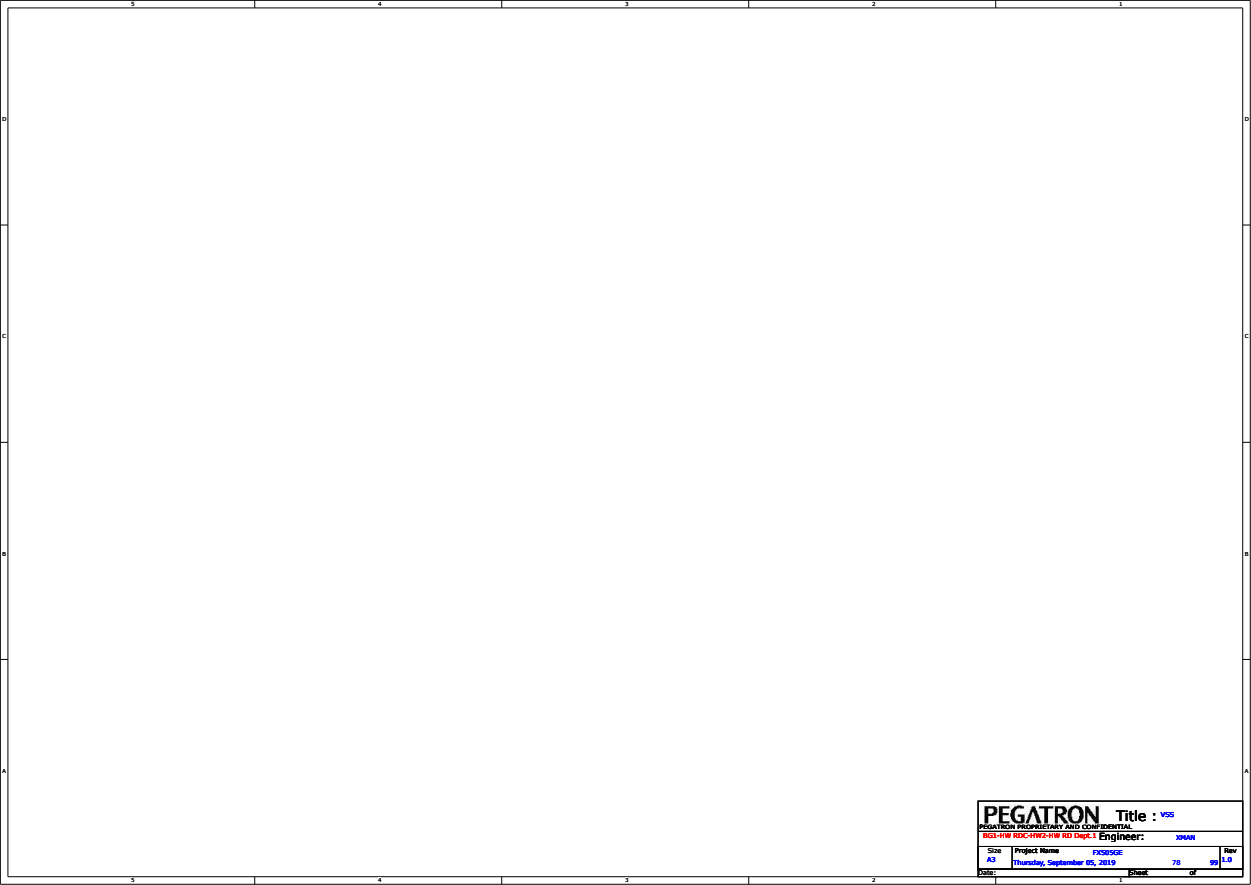


PEGATRON Title : VSS				
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dwg.1				
Engineer:			JOMAN	
Size	Project Name	FXSDSGE	Rev	
A3	Thursday, September 05, 2019	69	99	1.0
DATE		Sheet	of	
		1		

- ▶ N18E GPU does not support NVLink and SLI.
- ▶ Pull down NVHS_DVDD, NVHS_CVDD, NVHS_HVDD, and NVHS_PLL_HVDD rails to GND with 10 K resistor
- ▶ Do not use any decoupling or filtering capacitor for NVHS_DVDD, NVHS_CVDD, NVHS_HVDD, or NVHS_PLL_HVDD rails
- ▶ Leave NVHS_TERM_P, EXT_REFCLK_SLI, NVHS_REFCLK, NVHS_TX, and NVHS_RX signals floating (NC).

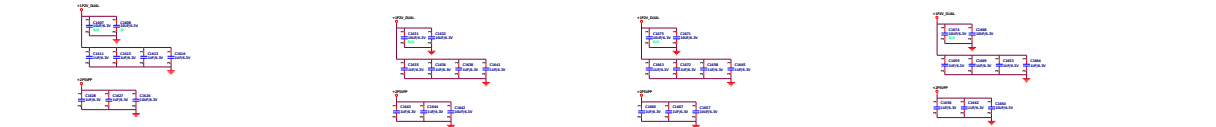
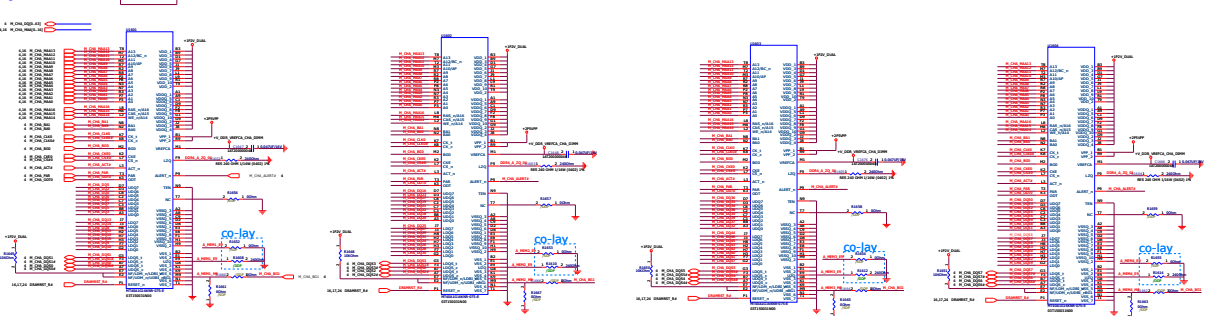
NVHS_DVDD, NVHS_HVDD, NVHS_PLL_HVDD can be pull to GND using 10K ohm, if no application





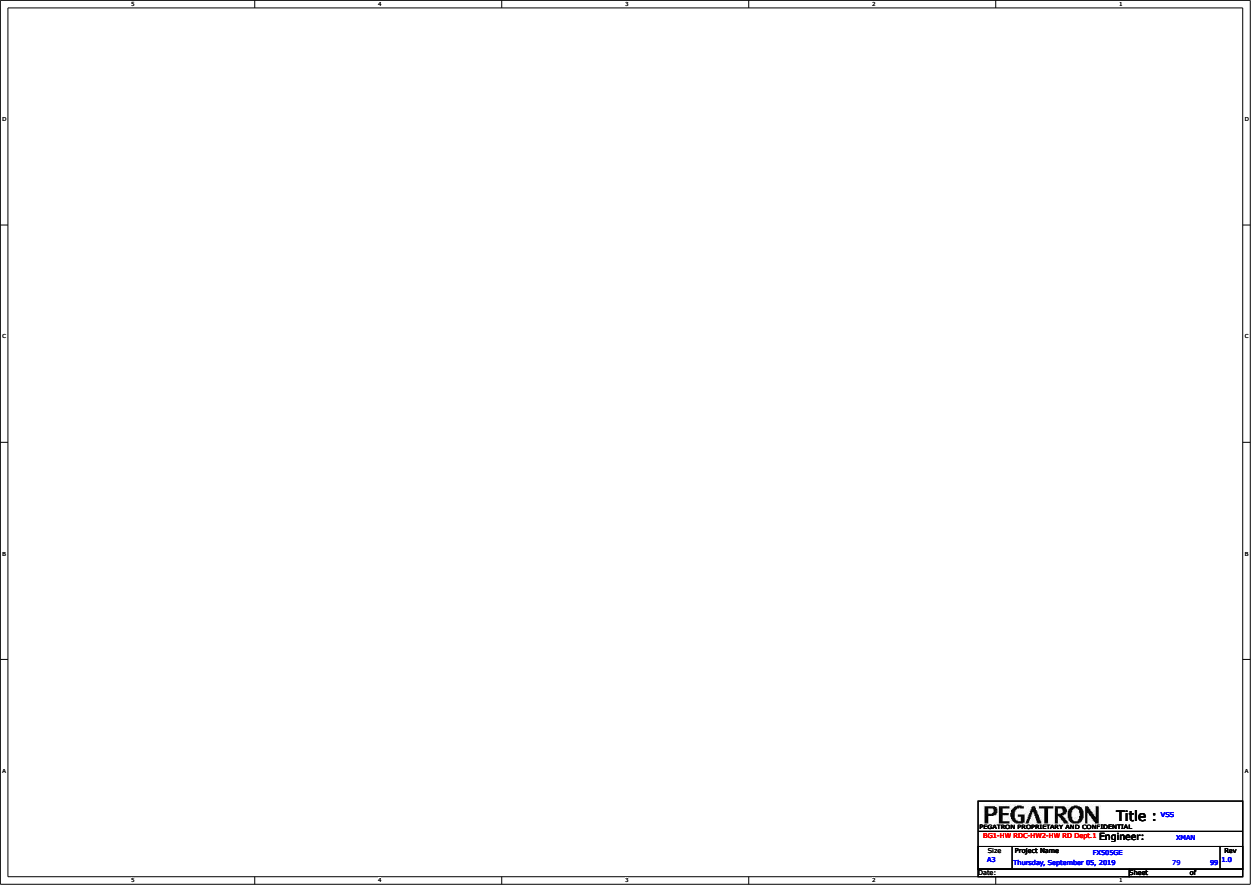
PEGATRON Title : VSS				
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dupr.1				
Engineer:			JOMAN	
Size	Project Name	FXSD5GSE		Rev
A3	Thursday, September 05, 2019	78	99	1.0
DATE		Sheet	of	
		1		

16 DDR4(1)_CH0



DDR4(0)_Termination



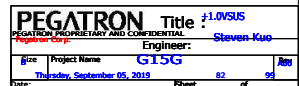


PEGATRON Title : VSS				
PEGATRON PROPRIETARY AND CONFIDENTIAL				
BG3-HW RDC-HW2-HW RD Dupr.1				
Engineer:			JOMAN	
Size	Project Name	FXSD5GE		Rev
A3	Thursday, September 05, 2019	79	99	1.0
DATE		Sheet	of	
		1		

(0.72A)

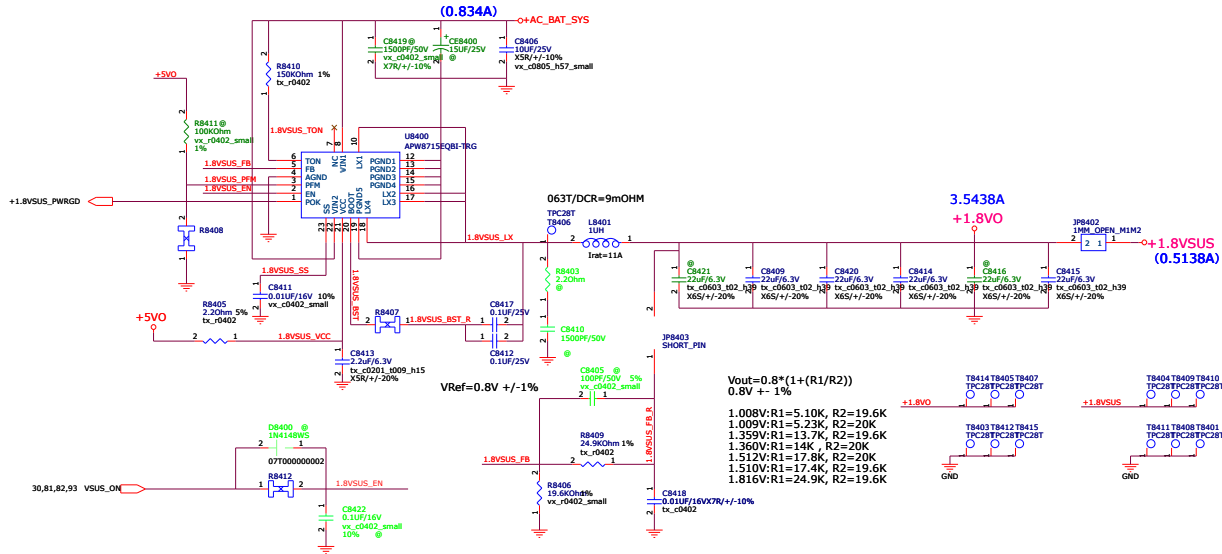
o+AC_BAT_SYS

201@ C8209 C8211 @
00PF/50V = 10UF/25V = 10UF/25V
c402_small X5R/+/-10% X5R/+/-10%
R/+/-10% vx_c0805_h57_small vx_c0805_h57_small

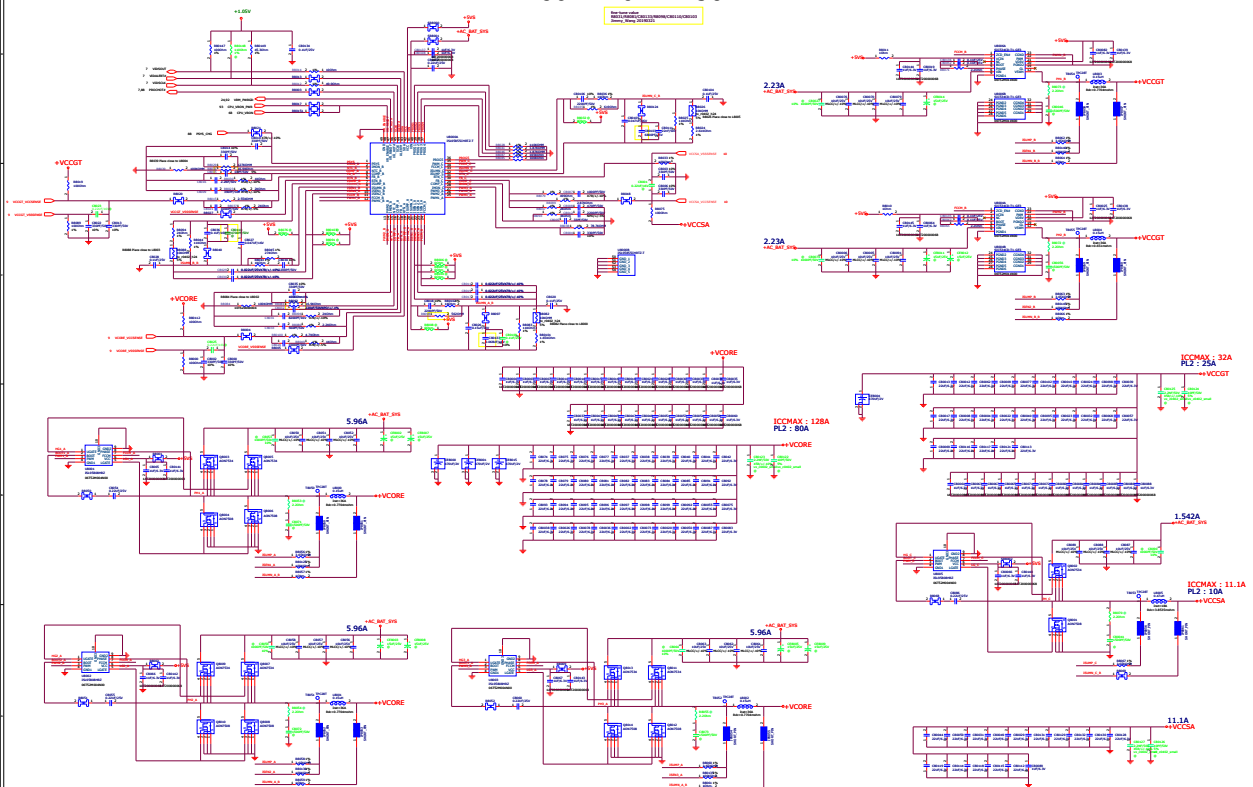


1.8VSUS POWER SUPPLY

換料APW8715E
Jimmy_Wang 20190225

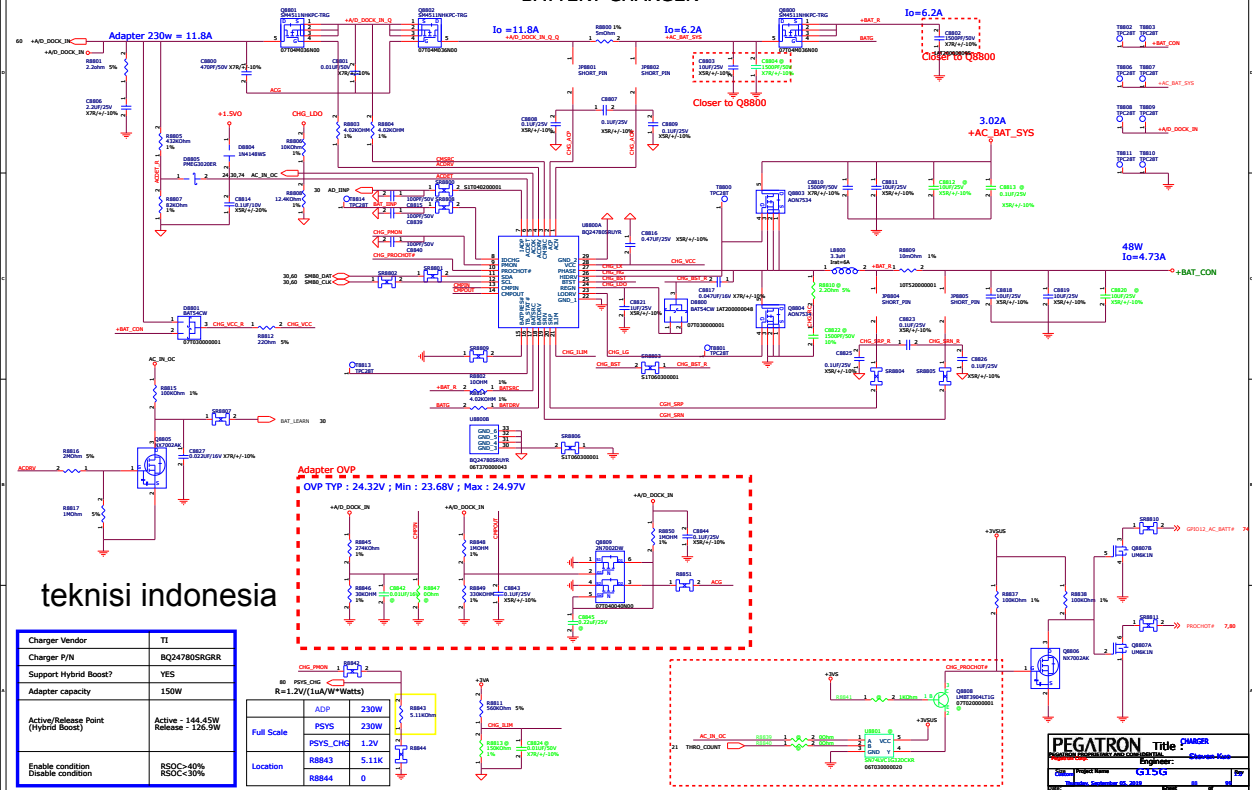


VCORE POWER SUPPLY



PEGATRON		Title : <u>41V8_A0N</u>	
PEGATRON PROPRIETARY AND CONFIDENTIAL		Engineer: <u>Steven-Kuo</u>	
Size	Project Name	Rev	
<u>615G</u>	<u>Thursday, September 05, 2019</u>	<u>86</u>	<u>99</u>
Date:		Sheet	of
<u>1</u>		<u>1</u>	<u>1</u>

BATTERY CHARGER

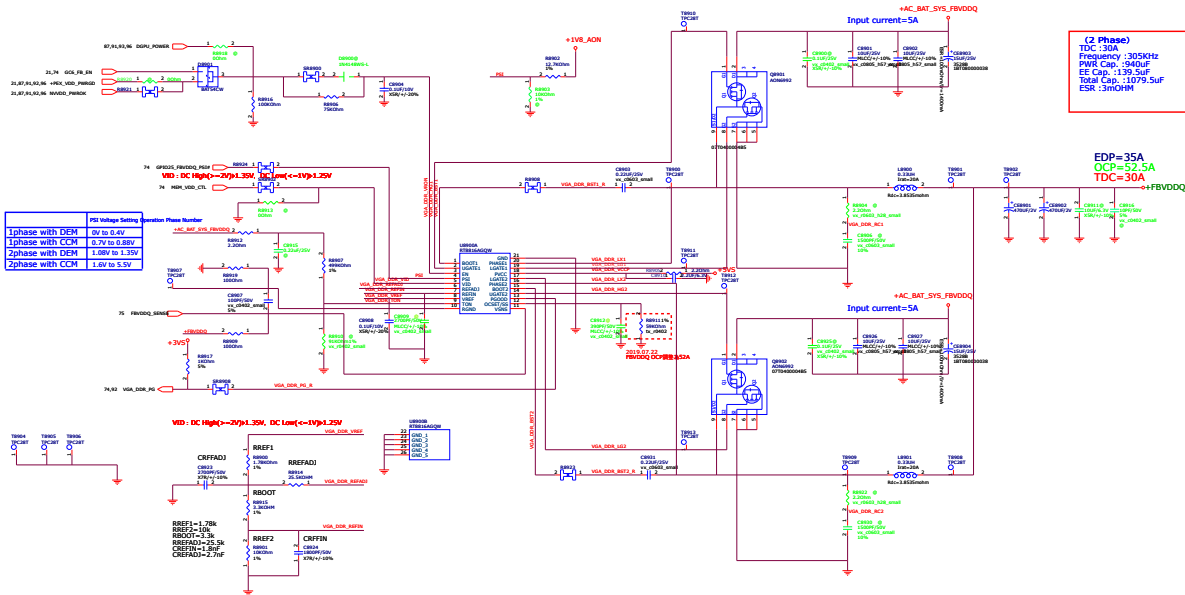


teknisi indonesia

Charger Vendor	TI
Charger P/N	BQ24780SRGR
Support Hybrid Boost?	YES
Adapter capacity	150W
Active/Release Point (Hybrid Boost)	Active - 144.45W Release - 126.9W
Enable condition Disable condition	RSOC>40% RSOC<30%

	ADP	230W
Full Scale	PSYS	230W
	PSYS_CHG	1.2V
Location	R8843	5.11K
	R8844	0

+FBVDDO POWER SUPPLY



(2 Phase)
TDC :30A
Frequency :305KHz
PWR Cap. :940uF
EE Cap. :139.5uF
Total Cap. :1079.5uF
ESR :3mOHM

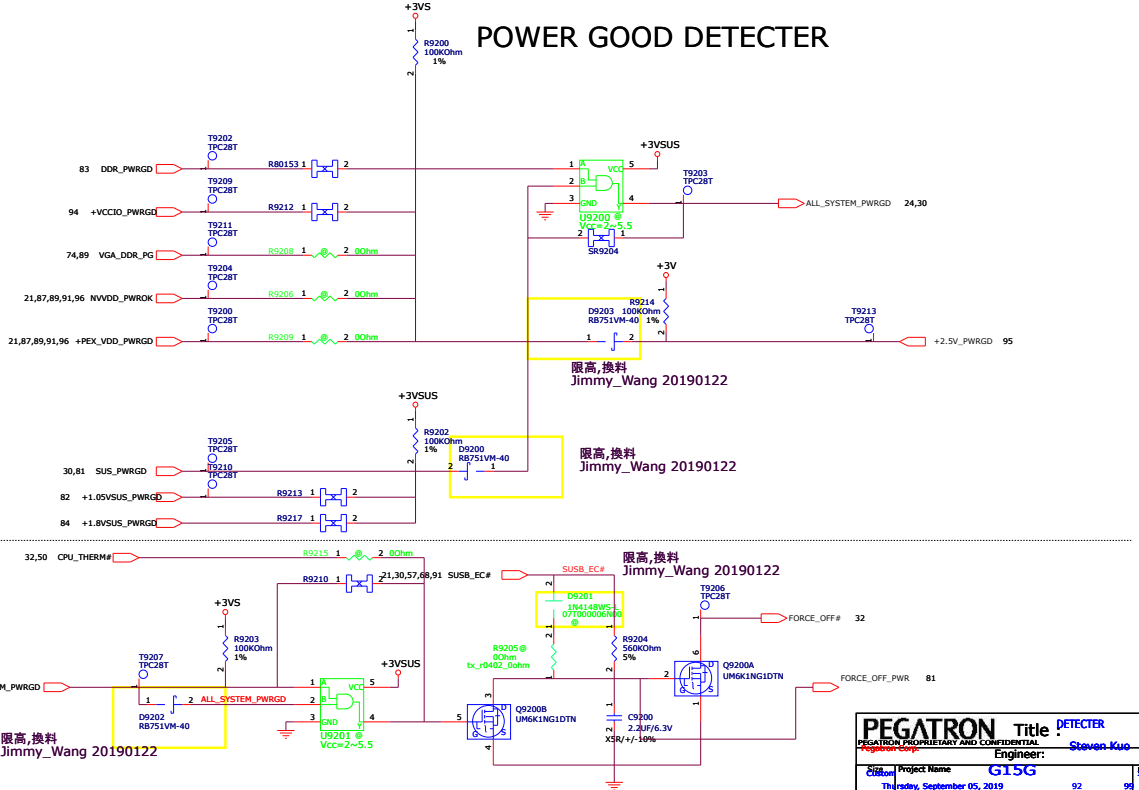
EDP=35A
OCP=52.5A
TDC=30A

PEGATRON		Title: DETECT	
PEGATRON, PEGATRONARY AND COMPASSION			
PEGATRONARY		Engineer: Steven-Kuo	
Project Name	GISG		By
Date:		90	99
Thursday, September 25, 2019		90	99

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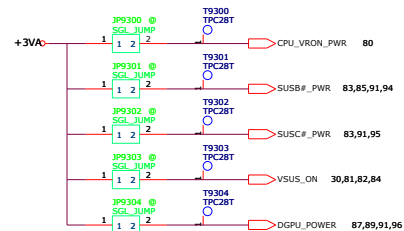


POWER GOOD DETECTOR



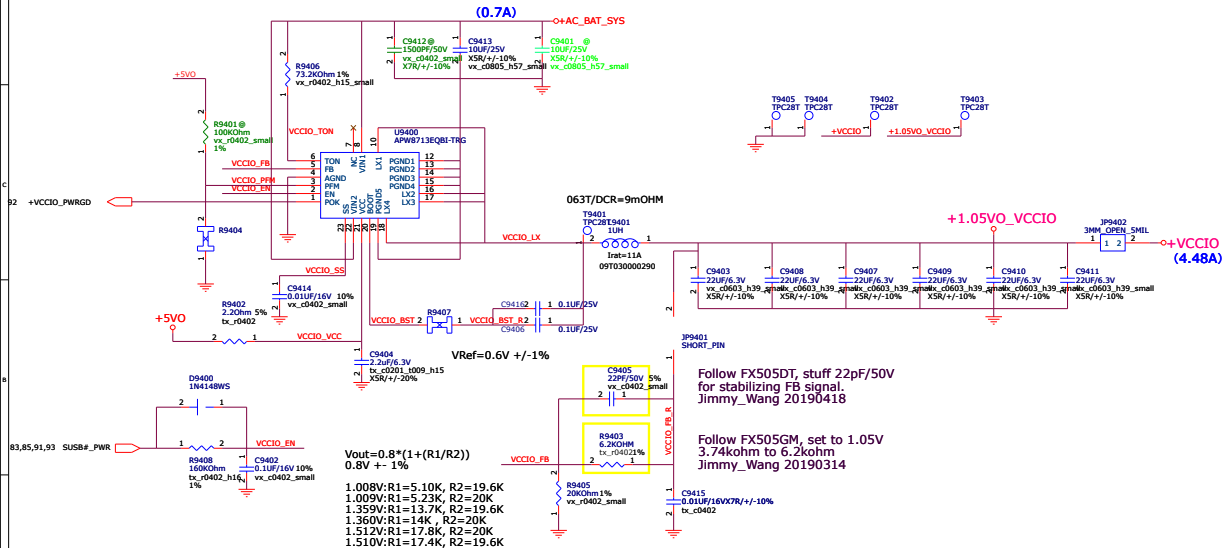
+A/D_DOCK_IN	→	+A/D_DOCK_IN	60,88
+BAT_CON	→	+BAT_CON	60,88
+AC_BAT_SYS	→	+AC_BAT_SYS	45,80,81,82,83,84,88,94,97
+12VSUS	→	+12VSUS	81,91
+3VO	→	+3VO	81,85,91,95
+3VSUS	→	+3VSUS	7,21,22,23,24,26,28,30,31,33,36,44,48,53,68,74,81,88,92,96
+3V	→	+3V	24,57,68,91,92
+3VS	→	+3VS	7,17,21,22,23,24,28,30,31,32,33,36,44,45,48,50,51,57,74,87,88,89,91,92,96
+3VS_VGA	→	+3VS_VGA	57,74,91,97
+3VA	→	+3VA	25,30,57,66,74,81,88,97
+5VO	→	+5VO	81,82,83,84,91,94,95,96
+5VSUS	→	+5VSUS	31,56,81
+5V	→	+5V	7,52,57,91
+5VS	→	+5VS	36,48,50,51,56,57,80,87,89,91
+1.05VO	→	+1.05VO	82,91
+1.05VSUS	→	+1.05VSUS	26,82
+1.05V	→	+1.05V	7,10,24,32,57,80,91
+1.05VS	→	+1.05VS	7,10,57,91
+1P2V	→	+1P2V	7,10,16,17,18,24,57,83
+0.6VO	→	+0.6VO	83
+VTT_DDR	→	+VTT_DDR	17,18,57,83
+1.8VO	→	+1.8VO	84,91
+1.8VSUS	→	+1.8VSUS	21,26,53,84
+1VB_MAIN	→	+1VB_MAIN	48,57,70,71,72,74,91
+1VB_AON	→	+1VB_AON	57,70,72,74,75,76,77,87,89,91
+1.05VO_VCCIO	→	+1.05VO_VCCIO	
+VCCIO	→	+VCCIO	3,6,7,10,94
+2.5VO	→	+2.5VO	95
+2PSVPP	→	+2PSVPP	16,17,18,57,95
+PEX_VDD	→	+PEX_VDD	57,70,72,73,96
+NVVDD	→	+NVVDD	57,75,87
+FBVDDQ	→	+FBVDDQ	57,71,75,76,77,89
+VCORE	→	+VCORE	9,80
+VCCGT	→	+VCCGT	9,80
+VCCSA	→	+VCCSA	10,80

FOR POWER TEST

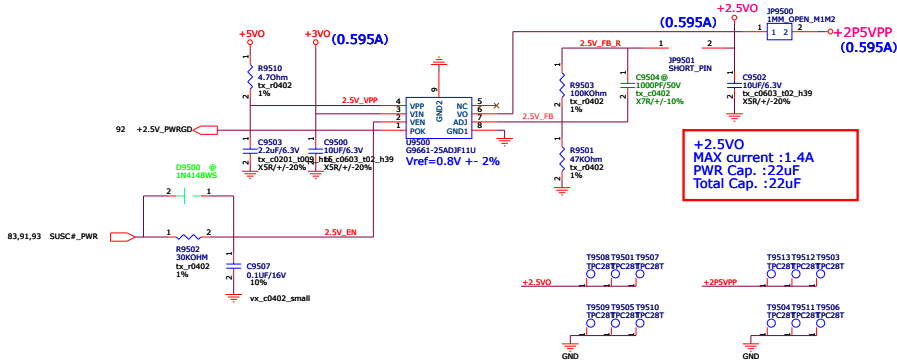


PEGATRON		Title	Signal
PEGATRON PROPRIETARY AND CONFIDENTIAL		Steven Kuo	
Pegatron Corp.		Engineer:	
Size	Project Name	G15G	Rev
Custom	Thursday, September 05, 2019	93	94
Date:	Thursday, September 05, 2019	Sheet	of

+VCCIO POWER SUPPLY

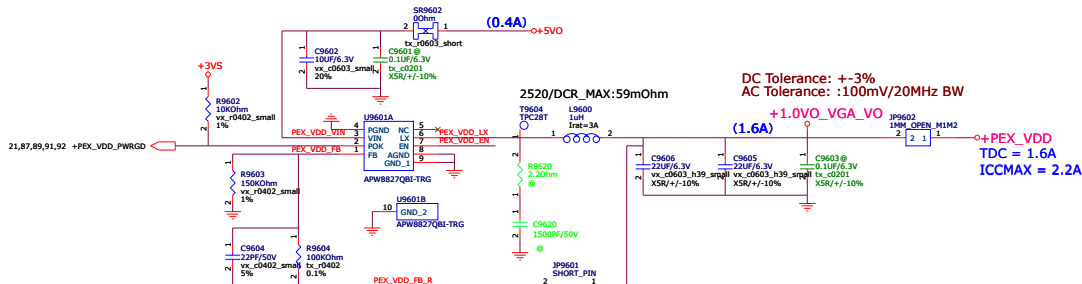


+2.5V POWER SUPPLY



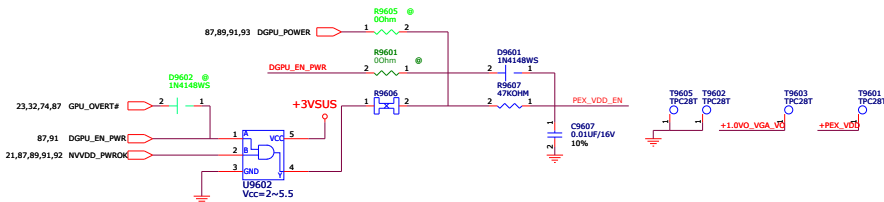
+PEX_VDD POWER SUPPLY

Page96 change solution
G9661 to APW8827 for rising time issue
Jimmy_Wang 20190315

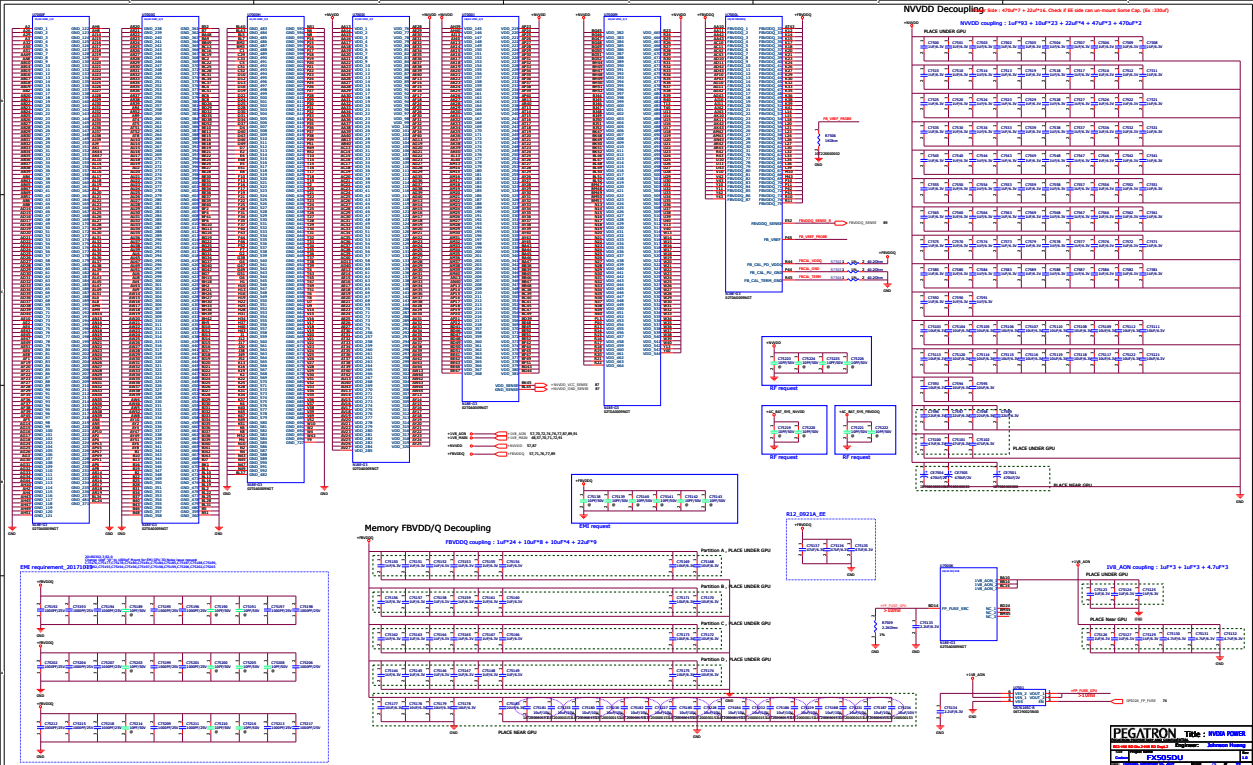


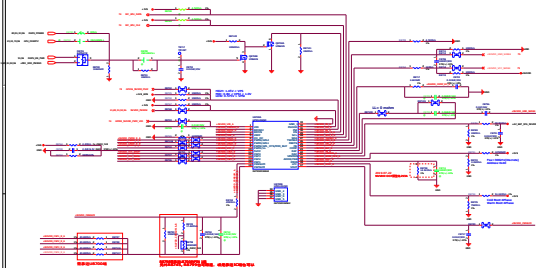
$$V_{out} = V_B * (1 + (R_{8509}/R_{8508}))$$

$$V_B = 0.6V; T = 1.5\%$$

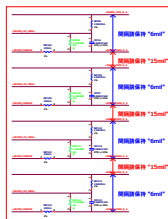


A	20190709C Remove parts of I7inch option and the resistors of 15" KB Option of I75inch is changed to N/A Remove jumper of I72V 20190710A Remove one 10pF and two 1uF per dram at p16 change 0.1uF to 1uF for capacitors connecting to vpp Remove the capacitors of P18 for CHA Add R1660~R1667 Remove R0401, R0402 Add R0512 and changed option of R0504 C0601~C0632 are changed to R001 20190710B All 1uF of page 16 are changed to 0201 Update power circuits: 1. Remove JP8302, JP8305, JP8306, JP8307, CE8006, CE8010 2. D8805 is changed to 07703000240 3. R8807 is changed to 82kohm 4. C8411 is changed to 1AT200000019 20190711A PEG reverse 0901-01UT000 is changed to 09T010002100 0315-02PY000 is changed to 03T150031N00 Update 09T0500000001 for system Update power circuits: Change PEX_VDD solution 20190711B Q4806 is changed to 077040000202 C5010 and C5002 are changed to 1AT300000019 U3608 is changed to 0718-01R0300 20190712A L4510 is recalled 0770300000113 is changed to 0770300026N00 077030000001 is recalled 0770000000002 is changed to 0770000006N00 96T2900000002 is recalled 1AT6000000002 is recalled Update power circuits: Return PEX_VDD solution 20190712B Remove PCB_ID0, PCB_ID5~PCB_ID7 0901-01H0000 is changed to 09T010005S00 H6514 and H6515 are changed to T-SH00000988 remove the ciruits of IFPA8_RSET, IFPA8_PLVDD, IFPE_RSET, IFPE_PLVDD Add C724 Remove R2424, T2417, T2412, T2401, T2404, T2425, Q2404, Q2412, Q2403, Q2420, R2402, R2403, R2408, D2402 Unmount C7109, R2458, R2459, R2464, Q2419 20190715A Remove R4401, R4403, R4406~R4409 Unmount R27423, R2744, R2475, C2412, Q2413, Q2414 D3611 is connected to A608 R3615, R3630~R3632, R3634, SR3601 are changed to 0ohm R0302 is changed to 20kohm Remove U0701, U0702, C0701, C0702 Remove C1025, C1026, C1028~C1030 R2138 is connected to VGA_D0R_PG R2146 is changed to 0ohm Remove U2101, R2143, R2144, R2156 Add T2126 20190715B Remove Q2413, Q2414, R2423, R2429, R2434, R2475, R2406, C2412 20190716A Swap Q5713A and Q5712 and unmount Q5712, R5723 for cost down R5728 is changed to 220ohm R5706 is changed to 100ohm and unmount R5718, Q5710 Remove Q2101, R2167, R2168 Remove T3059 Remove U2401, U2402, D2401, D2402, Q2401 R2407, R2422, R2423, R2459, R2467, R2478, R2479 R2417 is changed to 330kohm Swap memory Unmount H6522 Add R9130 Unmount C2620 and mount C2638 Remove R0611~R0613, R2640, R2649, R2621, R2624, R2633, R2635~R2639, R2641, R2642, SP2601 Add R2399 and reserve R2169 20190717A CONS301 is changed to 1274400005N00 1AT1000010900 and 1AT2000000284 are changed to 1AT200000230 for sourcer request Remove U6802, U6803 Mount R2458, R2459 Update power circuits: Add D8104 R8088, R8082, R8026 are changed to 10T540000002 20190718A Update block diagram Reserve CS322 for EMC request Remove TS102, TS103 Remove R5014 and +FAN is changed to +5VS 20190719A memory swap CMC and RM swap 20190719B Remove JP5101 and add JP5102, JP5103 Swap PCIEG_TXN1 and PCIEG_TXP1 Swap CH3302 20190719C Update power circuits: R8094 is changed to 10T2200000052 R80101 is changed to 10T2200000052 R8087 is changed to 10T2200000273 R8052 is changed to 10T220003348 C8032 is changed to 1AT200000100 R80100 is changed to 10T2200000062 C8034 is changed to 1AT200220V00 C8026 is changed to 1AT200641V00 R8045 is changed to 10T220000195 R8030 is changed to 10T220000002 R8015 is changed to 10T220000115 R8021 is changed to 1AT200220V00 R8099 is changed to 10T220000197 R8053 is changed to 10T220000232 20190722A NVVDD_PWR0K_R is changed to GPU_PWR0K +5V_KB is changed to +5VSUS_KB N129963392 is changed to +5VS_VPDD Update power circuits: R8102 is changed to 10T220000118 R8103 is changed to 10T220000367 R8911 is changed to 10T220000156 R8302 is changed to 10T220000472 R8745 is changed to 10T220000138 C8712 is changed to 10T2200000021 R8706, R87103, R87110, R87113 are changed to 10T220000453 Remove R87122 20190723A T-00000197 is changed to S1T040205MIL T-00000198 is changed to S1T1042020001 SP7402 is changed to SP1702 R2805~R2807, R2814~R2816 are changed to 0ohm 20190724A H6516 is changed to T-SH000005988 20190724B C2612 and 2619 are changed to 0402 size for height problem 20190725A Add net name: H_TRIGOUT_CPU 20190725B PR CM3504 is changed to CM3404 20190729A CM33102, R3069, R3163 are changed to @ R7217~R7219 are changed to @ 20190808A Unmount Q5704, R5716, R5735 Optional of R2230, R2231, R2233 are changed Update power circuits: R9502 is changed to 30kohm 20190823A Remove T7500 20190829A Remove R4502 Add R4507, R4508 20190902A Mount CS322, C2405, C3105 for EMI request Add CS103, C3801 for EMI request Recall all the error parts for layout-system request 20190902B Part of 0ohm are changed to short pad(R2802, R3164, R7422) 20190903A Part of 0ohm are changed to short pad(R23601, R3619, R3630~R3632, R3634) Recall all the error parts for layout-system request 20190903B Update power circuits: Part of 0ohm are changed to short pad(R8305, R8412, R9130) Recall all the error parts for layout-system request R80101 is changed to 1.65kohm R80100 is changed to 4.7kohm R8092 is changed to 100kohm R8080 is changed to 2.2kohm R8094 is changed to 2kohm R8015 is changed to 2.55kohm R8029 is changed to 127kohm C80111 is changed to 22nF C80103 is changed to 6800pF	20190904A CONS301 is changed to 127440001N00 www.teknisi-indonesia.com





ESP-225A Rev5
DC-LEA
4/10/2020



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